IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

TexasLDPC Inc., Plaintiff, v. Broadcom Inc., Defendant.	C.A. No. **JURY TRIAL DEMANDED**

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff TexasLDPC Inc. (the "Plaintiff" or "TexasLDPC"), by and through its attorneys, for its Complaint for patent infringement against Broadcom Inc. (the "Defendant" or "Defendant Broadcom"), hereby allege as follows:

THE PARTIES

1. Plaintiff TexasLDPC Inc. is a Texas Corporation with its principal place of business located at 1920 W Villa Maria Rd #301, Bryan, Texas 77807.

2. On information and belief, Defendant Broadcom Inc. is a Delaware corporation with its principal place of business located at 1320 Ridder Park Drive San Jose, California 95131.

3. On information and belief, Defendant Broadcom Inc. conducts business operations throughout the United States, including in the State of Delaware.

4. On information and belief, LSI Corporation ("LSI") was a semiconductor and software design company based in San Jose, California.

5. On information and belief, LSI was acquired by Avago Technologies Ltd. ("Avago"), a Singapore Corporation, in 2014.

6. On information and belief, Avago acquired Broadcom Corporation, a California Corporation, in 2016, and adopted the name Broadcom Limited. On information and belief, Broadcom Limited was redomiciled in the United States as Broadcom Inc. in 2018. Defendant Broadcom Inc. is a designer, developer, and global supplier of products based on analog and digital semiconductor technologies.

7. On information and belief, Defendant Broadcom Inc. has assumed, *inter alia*, all liabilities and obligations of Broadcom Limited, Broadcom Corp., Avago, and LSI (hereinafter the "Broadcom Predecessor Entities").

JURISDICTION AND VENUE

8. Plaintiff's patent infringement claims arise under the Patent Laws of the United States, 35 U.S.C. §§ 100 *et seq*. This Court has jurisdiction over the subject matter of this action under 28 U.S.C. §§ 1331 and 1338(a).

9. Plaintiff's copyright infringement claims arise under the Copyright Laws of the United States, 17 U.S.C. §§ 101, *et seq*. This Court has exclusive subject matter jurisdiction over the copyright claims under 28 U.S.C. § 1331 and 1338 and 17 U.S.C. § 501(a).

10. This Court has personal jurisdiction over Defendant because Defendant is a Delaware corporation.

11. Defendant is registered to do business in the State of Delaware.

12. Corporation Service Company, 251 Little Falls Drive, Wilmington, DE 19808, serves as Defendant's Registered Agent in the State of Delaware.

13. The Court has personal jurisdiction over Defendant because Defendant is incorporated in this judicial district and because, on information and belief, Defendant has regularly and systematically transacted business in this judicial district, directly or through

intermediaries, and/or committed acts of infringement in this judicial district. Defendant has also placed infringing products into the stream of commerce by shipping those products into this district or knowing that the products would be shipped into this district.

14. Venue is proper in this judicial district pursuant to 28 U.S.C. §1400(b).

PATENTS-IN-SUIT

15. On August 9, 2013, United States Patent No. 8,418,023 ("the '023 Patent"), entitled "Low Density Parity Check Decoder For Irregular LDPC Codes," was duly and legally issued by the United States Patent and Trademark Office ("PTO"). A true and correct copy of the '023 Patent is attached as **Exhibit A** to this Complaint.

16. On October 8, 2013, United States Patent No. 8,555,140 ("the '140 Patent"), entitled "Low Density Parity Check Decoder For Irregular LDPC Codes," was duly and legally issued by the PTO. A true and correct copy of the '140 Patent is attached as **Exhibit B** to this Complaint.

17. On August 18, 2015, United States Patent No. 9,112,530 ("the '530 Patent"), entitled "Low Density Parity Check Decoder," was duly and legally issued by the PTO. A true and correct copy of the '530 Patent is attached as **Exhibit C** to this Complaint.

18. On January 22, 2013, United States Patent No. 8,359,522 ("the '522 Patent"), entitled "Low Density Parity Check Decoder For Regular LDPC Codes," was duly and legally issued by the PTO. A true and correct copy of the '522 Patent is attached as **Exhibit D** to this Complaint.

19. On February 18, 2014, United States Patent No. 8,656,250 ("the '250 Patent"), entitled "Low Density Parity Check Decoder For Irregular LDPC Codes," was duly and legally

issued by the PTO. A true and correct copy of the '250 Patent is attached as **Exhibit E** to this Complaint.

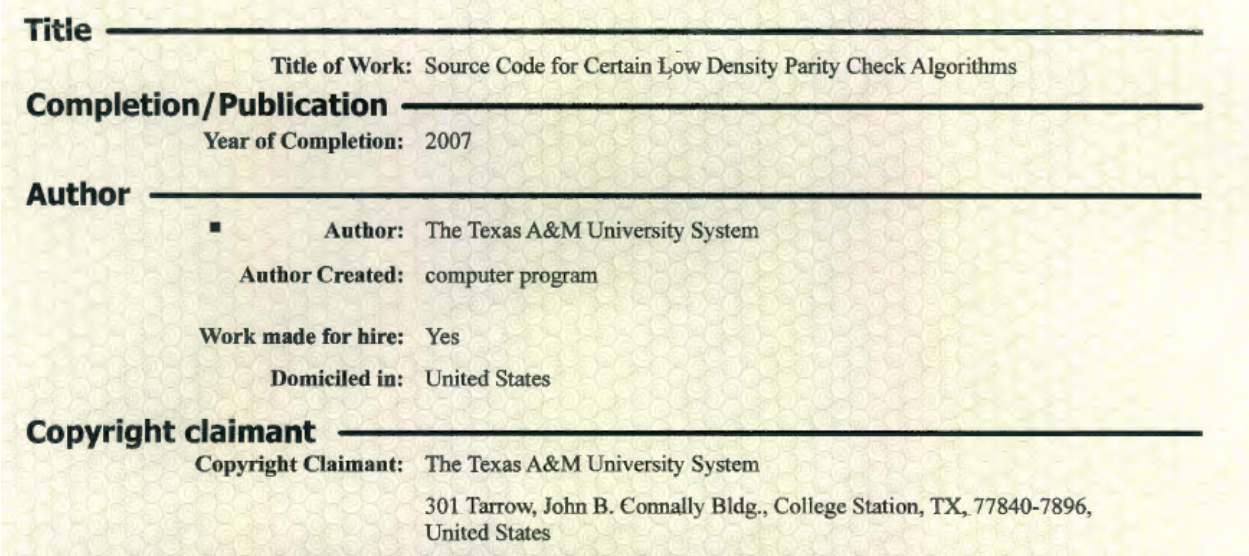
20. On November 27, 2018, United States Patent No. 10,141,950 ("the '950 Patent"), entitled "Low Density Parity Check Decoder," was duly and legally issued by the PTO. A true and correct copy of the '950 Patent is attached as **Exhibit F** to this Complaint.

21. The '023, '140, '530,'522, '250, and '950 Patents are collectively referred to herein as the "Patents-in-Suit."

22. The Patents-in-Suit are each assigned by their named inventors, Dr. Kiran Gunnam ("Dr. Gunnam"), and Dr. Gwan S. Choi, to the Texas A&M University System (TAMUS). Plaintiff is the exclusive licensee of each of the Patents-in-Suit pursuant to a license agreement between TAMUS and Plaintiff, executed on June 18, 2015 (the "TAMUS License Agreement"). Pursuant to the TAMUS License Agreement, Plaintiff has the exclusive and sole right (subject a pre-existing license) to practice the Patents-in-Suit, grant sub-licenses thereto, and sue and recover damages for the past, present, and future infringement of the Patents-in-Suit.

COPYRIGHTS-IN-SUIT

23. Dr. Gunnam, an employee of Texas A&M Engineering Experiment Station ("TEES"), a subdivision of TAMUS, working under the guidance and review from Dr. Choi, an employee of TEES, expended time, intellectual effort, and capital to create a computer program work entitled "Source Code for Certain Low Density Parity Check Algorithms" (the "LDPC Algorithms Source Code Work").



Title

Title of Work: Source Code for Certain Low Density Parity Check Algorithms

Completion/Publication

Year of Completion: 2007

Author

- **Author:** The Texas A&M University System

Author Created: computer program

Work made for hire: Yes

Domiciled in: United States

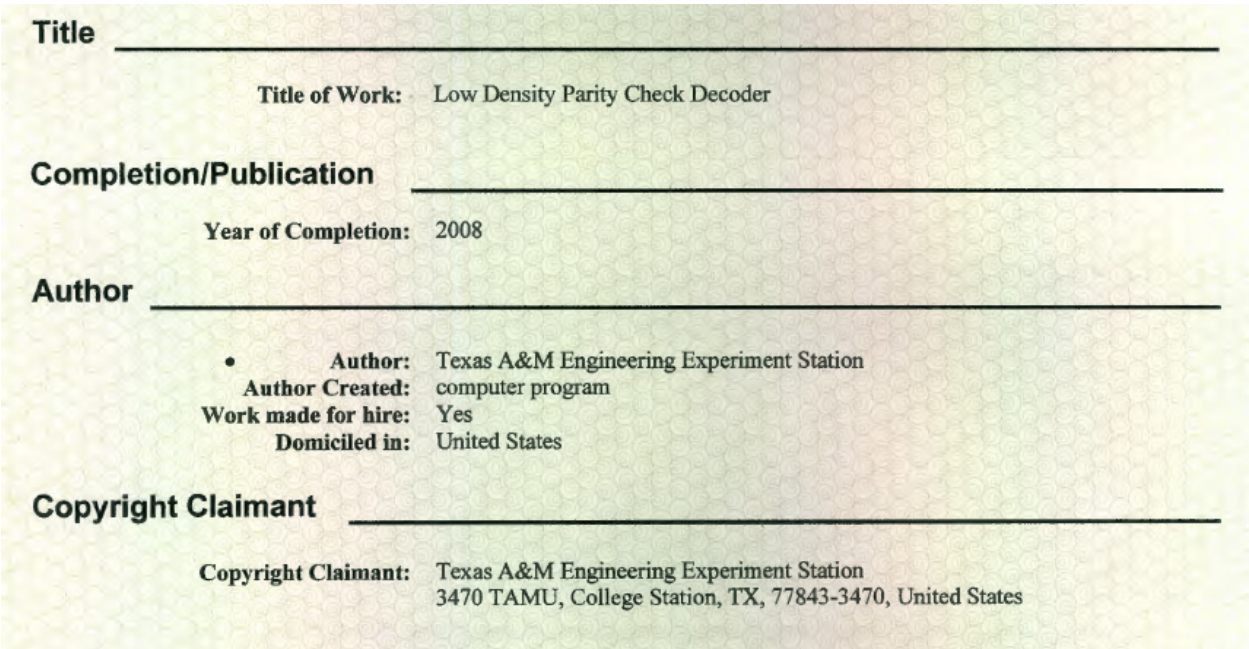
Copyright claimant

Copyright Claimant: The Texas A&M University System

301 Tarrow, John B. Connally Bldg., College Station, TX, 77840-7896, United States

24. As shown above, TAMUS registered its copyright in and to the LDPC Algorithms Source Code Work with the United States Copyright Office and was granted U.S. Copyright Registration No. TXu 1-842-620, which issued on February 11, 2013. Attached hereto as **Exhibit G** is a copy of Registration No. TXu 1-842-620.

25. Dr. Gunnam, an employee of TEES, a subdivision of TAMUS, working under the guidance and review from Dr. Choi, an employee of TEES, expended time, intellectual effort, and capital to create a computer program work entitled "Low Density Parity Check Decoder" (the "LDPC Decoder Program Work").



Title

Title of Work: Low Density Parity Check Decoder

Completion/Publication

Year of Completion: 2008

Author

- **Author:** Texas A&M Engineering Experiment Station
  Author Created: computer program
  Work made for hire: Yes
  Domiciled in: United States

Copyright Claimant

Copyright Claimant: Texas A&M Engineering Experiment Station
3470 TAMU, College Station, TX, 77843-3470, United States

26. As shown above, TEES registered its copyright in and to the LDPC Decoder Program Work with the United States Copyright Office and was granted U.S. Copyright Registration No. TXu 2-001-020, which issued on October 12, 2015. Attached hereto as **Exhibit H** is a copy of Registration No. TXu 2-001-020.

27. Dr. Gunnam, an employee of TEES, a subdivision of TAMUS, working under the guidance and review from Dr. Choi, an employee of TEES, expended time, intellectual effort, and capital to create a computer program work entitled "Source Code for Low Density Parity Check Decoder and Its Modules" (the "LDPC Decoder Source Code Work").

Title

Title of Work: Source Code for Low Density Parity Check Decoder and Its Modules

Completion/Publication

Year of Completion: 2007

Author

- **Author:** Texas A&M Engineering Experiment Station
  Author Created: computer program
  Work made for hire: Yes
  Domiciled in: United States

Copyright Claimant

Copyright Claimant: Texas A&M Engineering Experiment Station
3369 TAMU, College Station, TX, 77843-3369, United States

28. As shown above, TEES registered its copyright in and to the LDPC Decoder Source Code Work with the United States Copyright Office and was granted U.S. Copyright Registration No. TXu 2-033-302, which issued on November 29, 2016. Attached hereto as **Exhibit I** is a copy of Registration No. TXu 2-033-302.

29. Collectively TAMUS' LDPC Algorithm Source Code Work, LDPC Decoder Program Work, and LDPC Decoder Source Code Work constitute the "TAMUS Copyrighted Works." Pursuant to the TAMUS License Agreement, Plaintiff has been granted by TAMUS an exclusive license and right to reproduce, distribute, publicly display and perform, and make derivative works from the TAMUS Copyrighted Works, grant sublicenses thereto, and to sue for infringement of the copyrights in the TAMUS Copyrighted Works, including the exclusive right to collect damages for past, present, and future infringement of those copyrights.

30. The TAMUS Copyrighted Works were marked with copyright notifications informing any reader that the works were copyrighted – thus making any copying by Defendant willful.

31. Defendant and/or the Broadcom Predecessor Entities was also notified by Dr. Gunnam that the TAMUS Copyrighted Works were property of TAMUS and could not be copied or used without a license.

FACTUAL BACKGROUND

Development of the Patented Technology

32. Each of the Patents-in-Suit is directed to improved designs and methods for using low-density parity check code ("LDPC") decoders. LDPC decoders decode data that has been encoded using an LDPC code, a type of error correcting code. By encoding data in this fashion, digital electronic devices can transmit data over a noisy channel, while being able to detect and correct errors. As a result, such devices are able to operate at substantially higher data rates than would otherwise be possible.

33. The Patents-in-Suit improve upon prior LDPC decoder technology by providing decoder designs and techniques that are faster, more compact, and more energy efficient than prior art designs. These designs were developed by Dr. Kiran Gunnam, then a doctoral student at Texas A&M University (TAMU), working under the supervision of his thesis advisor, Prof. Gwan Choi. Dr. Gunnam and Prof. Choi discovered techniques to optimize the then-conventional algorithms and circuit architectures for LDPC decoders so that they used less memory and avoided redundant calculations. Dr. Gunnam and Prof. Choi first described aspects of their new design in a TAMU technical report entitled "A Low Power Architecture for Min-Sum Decoding of LDPC Codes," TAMU-ECE-2006-02 (the "Low Power Architecture" report), which is available at https://cesg.tamu.edu/techreports/, and issued in May, 2006.

34. Subsequent to the issuance of the Low Power Architecture report, Dr. Gunnam and Prof. Choi published and presented extensively about aspects and applications of their new LDPC decoder designs, including in the following publications and presentations:

- Gunnam, *et al.*, "VLSI Architectures for Layered Decoding for Irregular LDPC Codes of WiMax," 2007 IEEE International Conference on Communications (Glasgow, UK, June 2007).
- Gunnam, *et al.*, "Decoding of Quasi-cyclic LDPC Codes Using an On-the-Fly Computation," 2006 Asilomar Conference on Signals, Systems and Computers (Pacific Grove, CA, October 2006).
- Gunnam, "Area and Energy Efficient VLSI Architectures for Low-Density Party-Check Decoders Using On-the-Fly Computation, Ph.D Thesis, Texas A&M University, December, 2006.
- Gunnam, *et al.*, "VLSI Architectures for Turbo Decoding Message Passing Using Min-Sum for Rate-Compatible Array LDPC Codes," 2007 2nd Int'l Symposium on Wireless Pervasive Computing, (San Juan, PR, Feb. 2007).
- Gunnam, *et al.*, "Multi-Rate Layered Decoder Architecture for Block LDPC Codes of the IEEE 802.11n Wireless Standard." 2007 IEEE International Symposium on Circuits and Systems, (New Orleans, LA, May 2007).

35. On May 1, 2007, less than one year after the issuance of the Low Power Architecture report, Dr. Gunnam and Prof. Choi filed a provisional patent application with the United States Patent and Trademark Office ("USPTO"), bearing application number 60/915,320 (the "'320 provisional application"). Each of the Patents-in-suit claims priority to the '320

provisional application, and is therefore entitled to a priority date of at least as early as May 1, 2007.

Development of the Copyrighted Works

36. During the course of his doctoral research, Dr. Gunnam built and tested specific decoding algorithms, decoder scheduling algorithms, decoder hardware architecture, micro-architecture, and circuit designs that implement the teachings of the Patents-in-Suit. Dr. Gunnam created simulation models for these designs in MATLAB code, and design descriptions in RTL code, a hardware description language. Each of the TAMUS Copyrighted Works comprise MATLAB and RTL code reflecting Dr. Gunnam's circuit designs decoding algorithms, decoder scheduling algorithms, decoder hardware architecture, micro-architecture, and circuit designs.

Dr. Gunnam's Employment with LSI and LSI's Willful Infringement of the Patents-in-Suit and the TAMUS Copyrighted Works

37. Dr. Gunnam completed his doctoral work at TAMU in December, 2006. In January, 2008, Dr. Gunnam was hired by LSI to work on advanced LDPC decoder designs for the next generation of LSI's TrueStore hard disk drive (HDD) controller chips. LSI was aware of Dr. Gunnam's prior work on advanced designs in this area, and specifically hired him so that he could help them evaluate those designs for possible incorporation into their next generation of HDD controller chips.

38. Prior to and immediately upon arriving at LSI, Dr. Gunnam informed LSI that the advanced LDPC decoder designs that he had developed while at TAMU represented the intellectual property of TAMUS, and that LSI would need to obtain a license from TAMUS if LSI wished to exploit Dr. Gunnam's designs in a commercial product. At the time Dr. Gunnam joined LSI, the decoder design for the newest generation of HDD controllers, code named

Mamba, had been frozen, and Dr. Gunnam was eventually invited to work on a subsequent generation design, code named McLaren.

39. In order to help LSI evaluate whether his advanced LDPC decoder designs were suitable for use in the McLaren design, Dr. Gunnam provided LSI with simulation models and circuit design files that he had created while at TAMU, and which are components of the TAMUS Copyrighted Works. Dr. Gunnam provided these files to LSI with the express understanding that if LSI decided to use these designs, it would need to obtain a license from TAMUS.

40. Although LSI held licensing discussions with TAMUS in the 2008 time period, LSI refused TAMUS' licensing terms and did not obtain a license from TAMUS for Dr. Gunnam's advanced LDPC decoder designs.

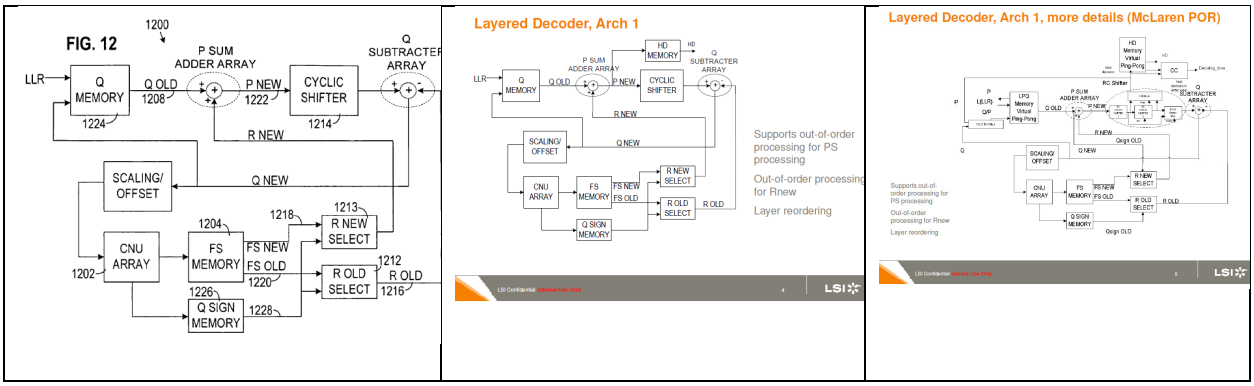
41. Despite not having obtained a license, LSI continued to investigate using Dr. Gunnam's LDPC decoder designs. In early 2009, Dr. Gunnam was assigned to work on the design of the McLaren LDPC decoder as the architect, under the supervision of Mr. Shaohua Yang and working closely with a design team led by Yen Johnson ("Mr. Johnson"). Also working under Mr. Johnson was Mr. Madhu Kalluri ("Mr. Kalluri"), a circuit designer. As part of the design process for the McLaren LDPC decoder, Mr. Kalluri worked with TAMUS RTL and MATLAB simulation files that had been provided to LSI by Dr. Gunnam, and that were part of the TAMUS Copyrighted Works. Mr. Johnson, Mr. Kalluri, and Dr. Gunnam were all aware that the simulation files were copyrighted by TAMUS and that LSI would need to obtain a license to use them.

42. Despite this knowledge, Mr. Kalluri was directed to rewrite the RTL code that had been provided by Dr. Gunnam, while maintaining the same basic program structure and

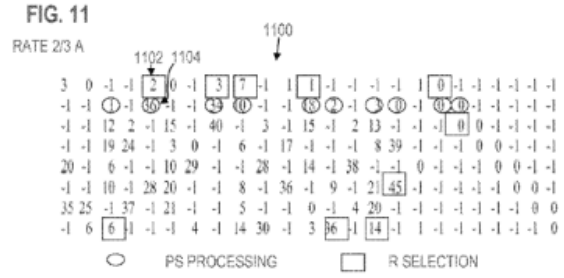
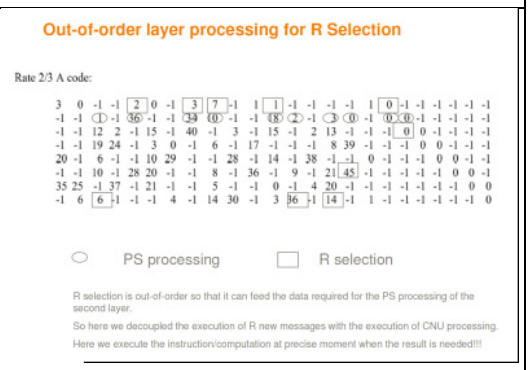
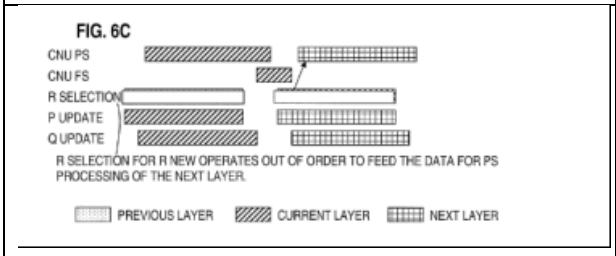
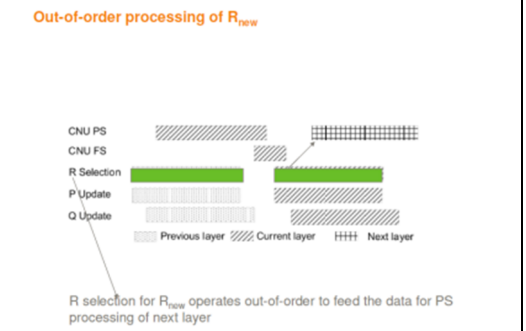
logic. In doing so, Mr. Kalluri at least created new design files that were derivative works of the TAMUS Copyrighted Works. Upon information and belief, LSI, and subsequently Defendant Broadcom, continued to use the TAMUS copyrighted and derivative works and make copies of them, throughout all of their subsequent design work for LDPC decoders used in HDD controllers.

43. In 2009 and 2010, Dr. Gunnam continued to work at LSI on the architecture for the McLaren LDPC decoder and, with LSI's knowledge and approval, incorporated key features from his advanced design work at TAMU into the LSI design. During this period, Dr. Gunnum repeatedly reminded LSI management of its obligation to obtain a license from TAMUS if it wished to use his designs.

44. On August 21, 2009, Dr. Gunnam created an internal LSI presentation entitled "Layered Decoder for LDPC Codes with Zero Matrices" (the "Zero Matrices Presentation"). A copy of this presentation is available on the internet at https://www.scribd.com/document/367470390/read-channel-overview-part-1. Dr. Gunnam's Zero Matrices Presentation described Dr. Gunnam's advanced architectural design for an LDPC Decoder developed at TAMU, a design that was essentially identical to the design in the then-pending patent applications that had been filed by Dr. Gunnam and Prof. Choi, which had been published by the USPTO on November 6, 2008 (Publication No. 2008/0276156A1, the "156 Publication"). The table below shows Figure 12 from the '156 Publication, the basic decoder architecture described in Dr. Gunnam's Zero Matrices Presentation, and a further elaboration of that design labelled as McLaren "POR" (Plan of Record).

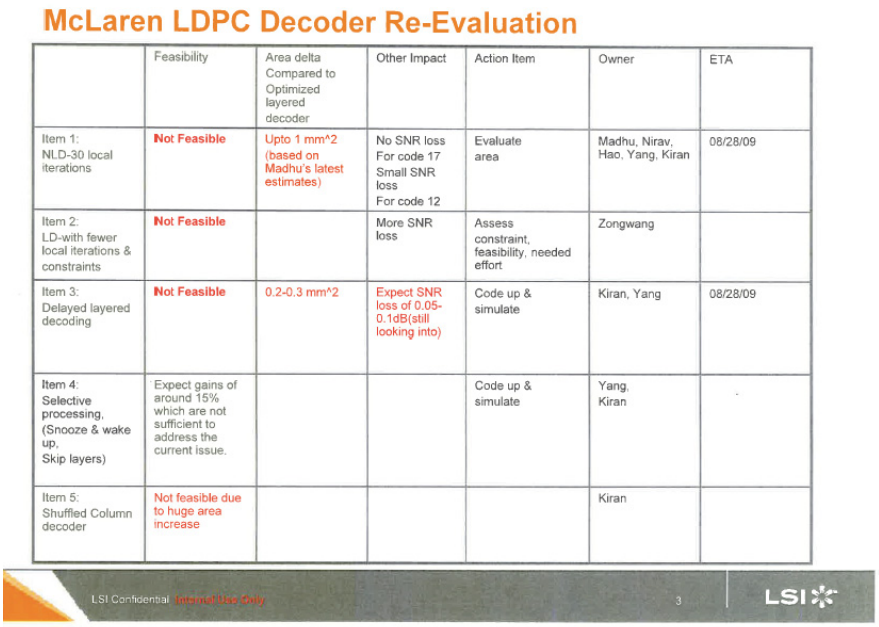


45. Dr. Gunnam's Zero Matrices Presentation included significant additional detail regarding the design of the LDPC decoder that was derived directly from the '156 Publication, as shown in the table below.

'156 Publication	Zero Matrices Presentation
	
	

46. On August 26, 2009, Dr. Gunnam, along with LSI colleagues Dr. Yan Hang and Mr. Kalluri, made a presentation entitled LDPC Decoder Reevaluation ("Reevaluation Presentation"). A copy of this presentation is available on the internet at https://www.scribd.com/document/367470390/read-channel-overview-part-1. The presentation explained that the "current option McLaren is the layered decoder with layer re-ordering and out-of-order processing," two key concepts from Dr. Gunnam's TAMU design. The presentation further stated that "we would like to re-evaluate the LDPC decoder options for McLaren due to non-technical issues." Upon information and belief, the "non-technical issues" that led to the re-evaluation of Dr. Gunnam's TAMU design was the understanding by LSI management that Dr. Gunnam's design was the subject of TAMUS pending patent applications and copyrights and that the use of that design would necessitate obtaining a license from TAMU.

47. The Reevaluation Presentation ("the presentation") described testing and modelling of five different alternatives to Dr. Gunnam's LDPC Decoder design. As shown in the table below, the presentation concluded that there were no viable alternatives to using Dr. Gunnam's design, and recommended staying with the existing design.



McLaren LDPC Decoder Re-Evaluation

	Feasibility	Area delta Compared to Optimized layered decoder	Other Impact	Action Item	Owner	ETA
Item 1: NLD-30 local iterations	Not Feasible	Upto 1 mm^2 (based on Madhu's latest estimates)	No SNR loss For code 17 Small SNR loss For code 12	Evaluate area	Madhu, Nirav, Hao, Yang, Kiran	08/28/09
Item 2: LD-with fewer local iterations & constraints	Not Feasible		More SNR loss	Assess constraint, feasibility, needed effort	Zongwang	
Item 3: Delayed layered decoding	Not Feasible	0.2-0.3 mm^2	Expect SNR loss of 0.05-0.1dB(still looking into)	Code up & simulate	Kiran, Yang	08/28/09
Item 4: Selective processing, (Snooze & wake up, Skip layers)	Expect gains of around 15% which are not sufficient to address the current issue.			Code up & simulate	Yang, Kiran	
Item 5: Shuffled Column decoder	Not feasible due to huge area increase				Kiran	

LSI Confidential Internal Use Only 3 LSI

48. In making its recommendation, the presentation noted that "other options have an area penalty of up to 1mm^2 or the SNR loss of more than 0.4dB." In other words, the other alternatives would take up more area, or would be less effective in correcting errors, than Dr. Gunnam's design. Upon information and belief, LSI considered those alternatives commercially unacceptable to Dr. Gunnam's design.

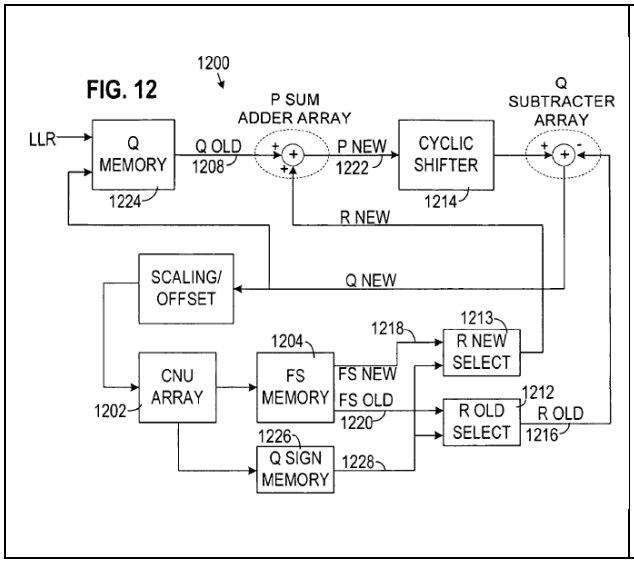
49. On October 13, 2009, an LSI team comprised of Dr. Gunnam, Dr. Zongwang Li, and Dr. Shaohua Yang made an internal presentation to LSI entitled "McLaren Client Server Architecture/Scheduling" ("Client Server Presentation"). A copy of this presentation is available on the internet at https://www.scribd.com/document/367470390/read-channel-overview-part-1. The Client Server Presentation, key features of the McLaren LDPC Decoder designs are discussed, and the decoder design is described as follows:

- New Decoder architecture: Use of layered decoder optimized based on "On-the-fly Computation" to minimize memory, logic requirements and remove the pipeline idle cycles and memory access conflicts associated with conventional layered/non-layered decoder designs. The decoder is highly optimized for area and high speed saving upto 1 mm^2 while compared to other implementations.

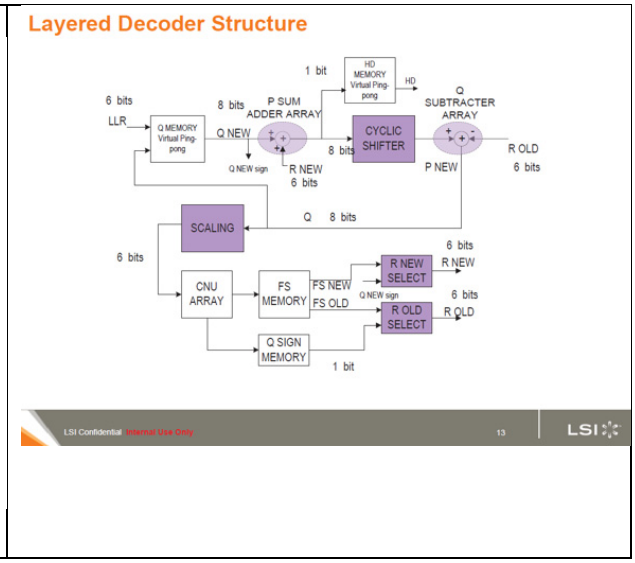
50. This description of the McLaren LDPC decoder included key features of the advanced decoder design developed by Dr. Gunnam at TAMU, including "on-the-fly computation to minimize memory, logic requirements and remove pipeline idle cycles and memory access conflicts associated with conventional layered/non-layered decoder designs."

51. Moreover, the architectural drawing included in the October 13, 2009 presentation was virtually identical to the corresponding drawing (Fig. 12) contained in specification of the Patents-in-Suit, a version of which had been published by the USPTO on November 6, 2008 (Publication No. 2008/0276156A1, the "'156 Publication").

'156 Publication at FIG. 12



LSI's Client Server Presentation



52. LSI management was extremely pleased with the work that Dr. Gunnam did on the LDPC decoder design for the McLaren chip. In his 2009 annual performance review, Dr. Gunnam's manager, Shaohua Yang, gave him an overall descriptor of "Exceeds Expectations," and stated as follows:

Kiran is the team member who worked hardest literally in the team around the clock. He has demonstrated the highest level of innovation in hardware architecture and decoder algorithm. the Mclaren codec hardware architecture and algorithm is a very smart architecture which sizes ~1mm2 less than any alternative than we have evaluated for the same LDPC code matrix. Kiran innovated the whole read path architecture and half of the write path architecture. The key inventions are the local-global interleaver architecture, layered decoder architecture, and codec integration.

Kiran also worked closely with more than 10 designers (in both Shanghai and Milpitas) on a hourly bases on various modules in the Mclaren channel. He has discovered hundreds of issues and addressed them during the early development stage.

53. Upon information and belief, LSI management finalized the design for the McLaren TrueStore HDD controller chip in 2010, and included patented features of Dr. Gunnam's LDPC decoder design in the final design. During 2010, Dr. Gunnam made repeated requests to LSI management to approach TAMUS to obtain a license for the TAMUS intellectual property that he knew to be incorporated into that design. LSI failed to act upon those requests and never obtained a license from TAMUS, despite its awareness at the time that at its McLaren design incorporated TAMUS intellectual property. LSI's actions caused Dr. Gunnam to become increasingly frustrated with LSI's failure to properly license the TAMUS intellectual property it was using in the McLaren design.

54. On December 21, 2010, Dr. Gunnam wrote an e-mail to certain managers at LSI entitled: "Some important legal and ethical issues." The e-mail pointed out that the LDPC decoder design used the McLaren design "reads on claims" in his and Dr. Choi's pending, published, patent applications, which, as discussed above, these certain managers were intimately familiar. Dr. Gunnam also stated that the layered decoder architecture proposed for Spyder, the code-name for the generation of HDD controller chips after McLaren, also read on claims in the pending applications. Dr. Gunnam's e-mail urged LSI to "look for a way to license the" pending patent applications. The email also notes that Dr. Gunnam had informed Mr. Shaohua Yang (now Director of Read Channel Backend Architecture at Broadcom) that LSI needed to attain a license from Texas A&M. The December 2010 email also stated that Dr.

Yang had informed Dr. Gunnam to refrain from listing the Texas A&M patent applications on LSI's internal wiki system related to the McLaren product.

55. In March of 2011, Dr. Gunnam was given his performance review for 2010. In this review, he was reprimanded for the December 21, 2010 e-mail because the e-mail supposedly "compromis[ed] the competitiveness of LSI's recent read channel [i.e., HDD controller] products by putting all possible/suspected IP infringements on record."

56. Shortly after receiving this review, Dr. Gunnam decided to leave his employment with LSI, and resigned in March, 2011.

57. After leaving LSI, Dr. Gunnam continued to be concerned that LSI was using TAMUS intellectual property without a license.

58. On April 27, 2012, Dr. Gunnam contacted Dr. Yuanxing Lee ("Dr. Lee"), Dr. George Mathew ("Dr. Mathew"), and Mr. Johnson Yen ("Mr. Yen") at their official LSI email addresses to inform them of the pending patent applications for the '023 and '522 patents.

59. At the time, Dr. Lee was a Vice President in charge of engineering at LSI, Dr. Mathew was a manager at LSI, and Mr. Yen was a senior engineering manager at LSI.

60. As part of this email, Dr. Gunnam again informed LSI that "claims read on several features of non-layered decoder and significant design of layered decoders (for the products I directly worked on as well as the products that are/being made based on my earlier work)."

61. Dr. Lee, Dr. Mathew, and Mr. Yen all received Dr. Gunnam's April 27, 2012 e-mail.

62. On information and belief, Dr. Lee called a meeting at LSI to discuss LSI's use of TAMUS' intellectual property in its products after receiving Dr. Gunnam's April 27, 2012 email. On information and belief, at least Dr. Lee and Mr. Madhusudan Kalluri attended this meeting.

63. On information and belief, LSI took no actions to stop LSI's infringement of the Patents-in-Suit after receiving Dr. Gunnam's April 27, 2012 email.

64. Thereafter, when the '522 Patent-in-Suit issued on January 22, 2013, Dr. Gunnam wrote an e-mail to Dr. Lee, Dr. Mathew, and Mr. Yen, notifying them the patent had issued, and that it covered several features of several implemented LSI decoders, including McLaren and Spyder.

65. Dr. Lee, Dr. Mathew, and Mr. Yen received Dr. Gunnam's January 22, 2013 e-mail.

66. None of these individuals acknowledged Dr. Gunnam's email, nor, upon information and belief, did they take any actions to ensure that the McLaren and Spyder chips were not infringing the '522 Patent-in-Suit.

67. On information and belief, LSI took no actions to stop LSI's infringement of the Patents-in-Suit after receiving Dr. Gunnam's January 22, 2013 email.

68. On January 31, 2014, Dr. Gunnam wrote again to Dr. Lee, informing him that the '023 and '140 Patents-in-suit had issued, and that the '250 patent was about to issue on February 18, 2014.

69. In that January 31, 2014 email, Dr. Gunnam reminded Dr. Lee that he had repeatedly discussed with him and other LSI managers over the years that the TAMUS patents disclose key features of LDPC decoders that had been incorporated into LSI's designs, that those decoder designs were "based on the material from these patents and patent applications," and

that "the issued and pending patents cover several features of several implemented and planned layered and non-layered decoders as part of the read channel ICs [i.e., the McLaren and Spyder disk controller chips]." Dr. Gunnam specifically identified claims 1-98 of the '522 patent, claims 1-30 of the '023 patent, claims 1-22 of the '140 patent, and claims 1-54 of the soon-to-issue '250 patent as covering features in the McLaren and Spyder products.

70. In the January 21, 2014 email to Dr. Lee, Dr. Gunnam also informed him that RTL code used by LSI to develop its LDPC decoder designs was based on TAMUS RTL code (which is a part of the TAMUS Copyrighted Works) and had similar structure, sequence, organization, and variables to that code. Dr. Gunnam advised Dr. Lee that this use of TAMUS RTL code could create a "copyright issue" for LSI.

71. Dr. Lee took no actions to stop LSI's use of Texas A&M's source code after receiving Dr. Gunnam's January 21, 2014 email.

72. Dr. Lee received Dr. Gunnam's January 31, 2014 e-mail.

73. On information and belief, LSI took no actions to stop LSI's infringement of the Patents-in-Suit after receiving Dr. Gunnam's January 31, 2014 email.

74. On information and belief, LSI, Avago, and now Defendant Broadcom Inc. have taken no efforts to cease or mitigate infringement of the Patents-in-Suit or the Copyrights-in-Suit.

Defendant applies the Texas A&M Technology to SSD Controller Products

75. In January 2012, LSI acquired SandForce, Inc, a maker of solid state drive ("SSD") controller products.

76. In 2014, LSI introduced Sandforce controllers using LSI's SHIELD technology.

77. In 2014, Mr. Kent Smith ("Mr. Smith"), an employee of LSI's Flash Components Division gave an interview (available at https://www.electronicdesign.com/memory/interview-kent-smith-addresses-error-correction-and-flash-storage-technology).

78. While being interviewed in 2014, Mr. Smith stated the following: "LSI's first implementation of LDPC codes was to correct errors in the magnet media of hard disk drives. LSI TrueStore read channels with LDPC iterative decoding technology have been shipping in high volume for HDDs since 2010. This experience and engineering expertise are leveraged in SHIELD error correction technology."

79. On information and belief, LSI incorporated features of the McLaren LDPC decoder design that are derived from, and covered by, the TAMUS Patents-in-suit into Sandforce Controllers at least by 2013, including at least the SandForce SF3700 flash controller family and other SandForce controllers with SHEILD technology ("the Accused SandForce Products").

80. On information and belief, LSI sold its SandForce line to Seagate in late 2014.

81. Sales of the SandForce SF3700 prior to this sale were made after LSI (now Broadcom Inc.) received notice of at least the '522 patent and had knowledge of their infringement of it.

82. On information and belief, Defendant acquired Densbits, Inc. in December 2015.

83. On information and belief, Densbits designs and manufactures SSD controller products.

84. On information and belief, following Defendant's acquisition of Densbits, Defendant assigned several individuals associated with the development of LSI's TrueStore products to work on improving the SSD controller technology purchased from Densbits.

85. On information and belief, Defendant has incorporated features of the McLaren LDPC decoder design that are covered by the TAMUS Patents-in-suit into Densbits' SSD controllers (the "Accused Densbits Products") and sold them to customers.

Defendant applies the Texas A&M Technology to WiFi Products

86. United States Patent No. 8,341,488, entitled "Accumulating LDPC (low density parity check decoder (the '488 patent") issued on December 25, 2012, and is assigned to Broadcom Corporation, one of the Broadcom Predecessor Entities. The named inventors are Andrew J. Blanksby and Alvin Lai Lin.

87. The '488 patent describes an LDPC decoder architecture that would, if operated, practice the inventions described in claims 62 to 84 of the '522 patent, and claims 17 to 40 of the '250 patent.

88. Andrew J. Blanksby holds the title of Distinguished Engineer at Broadcom Inc., and his LinkedIn page states that he "lead [sic] development of Low-Density Parity-Check (LDPC) technology for WLAN used in all major smart phones, tablets, and access points by companies such as Apple, Samsung, and LG."

89. Wi-Fi IEEE standards 802.11ac and 802.11ad support LDPC coding and decoding, and Wi-Fi chipsets sold by Broadcom must support LDPC decoding.

90. Upon information and belief, Broadcom chipsets that support 802.11ac and 802.11ad (hereinafter the "Accused Wi-Fi Products") incorporate designs from the '488 patent, and therefore infringe claims 62 to 84 of the '522 patent and claims 17 to 40 of the '250 patent.

91. The Accused Hard Disk Controller Products, the Accused SandForce Products, the Accused Densbits Products, and the Accused Wi-Fi Products are collectively referred to as the "Accused Products."

COUNT I
(Infringement under 35 U.S.C. § 271 of U.S. Patent No. 8,418,023)

92. Plaintiff repeats and re-alleges the paragraphs above as if fully set forth herein.

93. The '023 patent is valid, enforceable, and was duly issued on August 9, 2013 in full compliance with Title 35 of the United States Code.

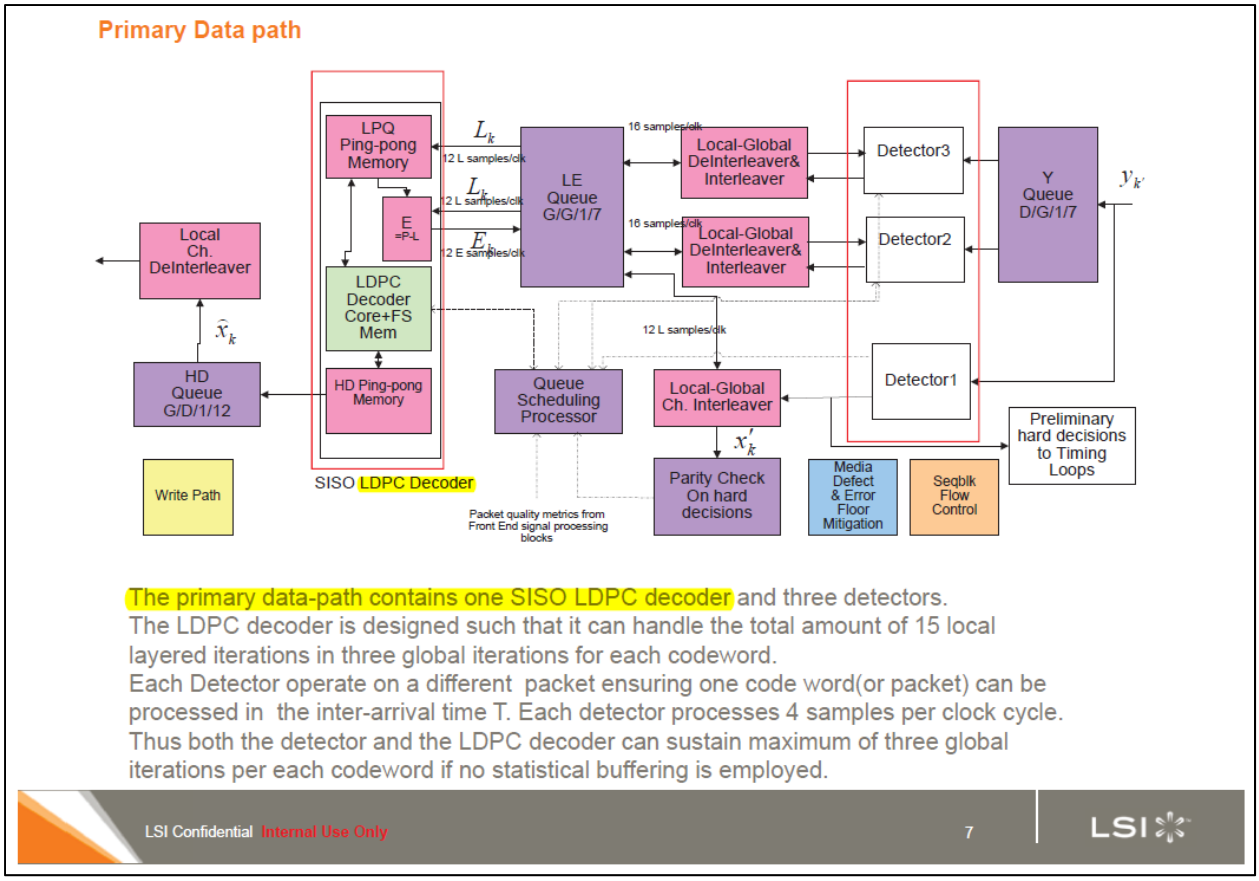
94. On information and belief, in violation of 35 U.S.C. § 271, Defendant and/or the Broadcom Predecessor Entities have infringed, contributed to the infringement of, and/or induced others to infringe the '023 patent, either literally or under the doctrine of equivalents, by, among other things, making, using, offering for sale, selling, and/or importing into the United States unlicensed systems and/or products in a manner that infringes Claims 1-30 of the '023 patent.

95. On information and belief, Defendant and/or the Broadcom Predecessor Entities have directly infringed the '023 patent, for example, by making, using, selling, offering to sell, and/or importing into the United States the Accused Products, which meet each and every limitation of at least Claim 1 of the '023 patent, in violation of Plaintiff's patent rights and without Plaintiff's license or authority. Non-limiting examples of such infringement are provided below, based on the limited information currently available to Plaintiff.

96. Claim 1 of the ’023 patent recites as follows:

> 1. A low density parity check code decoder, comprising:
> a control unit that controls decoder processing, the control unit configured to:
> cause the decoder to process blocks of a low density parity check (“LDPC”) matrix out of order; and
> schedule computation of R messages for a first non-zero block and computation of P messages and Q messages for a second non-zero block such that R messages for the first non-zero block are generated while processing the second non-zero block based on a determination of need for the R messages for the computation of P and Q messages for the second non-zero block;
> wherein the first non-zero block and the second non-zero block are in a same column of the matrix.

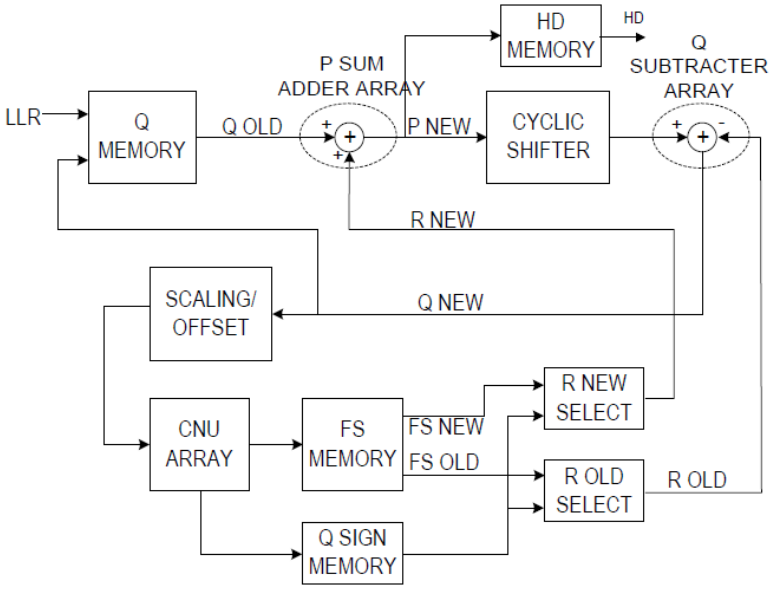
97. On information and belief, the Accused Products satisfy each and every limitation of Claim 1 of the ’023 patent. The Accused Products include a low density parity check code decoder. For example, an LSI presentation dated October 13, 2009 entitled: “Mclaren Client Server Architecture/Scheduling” (hereinafter, the “McLaren Architecture Presentation”) references the LDPC decoder.



98. The Accused Products include a control unit that controls decoder processing, and as set forth below, that control unit is configured to perform the actions required of the claimed control unit.

99. The Accused Products cause the decoder to process blocks of an LDPC matrix out of order. For example, an LSI presentation dated August 21, 2009 entitled: "Layered Decoder for LDPC Codes with Zero Matrices" (hereinafter, the "Layered Decoder Presentation") references out of order processing and includes many figures taken directly from the '023 patent.

Layered Decoder, Arch 1

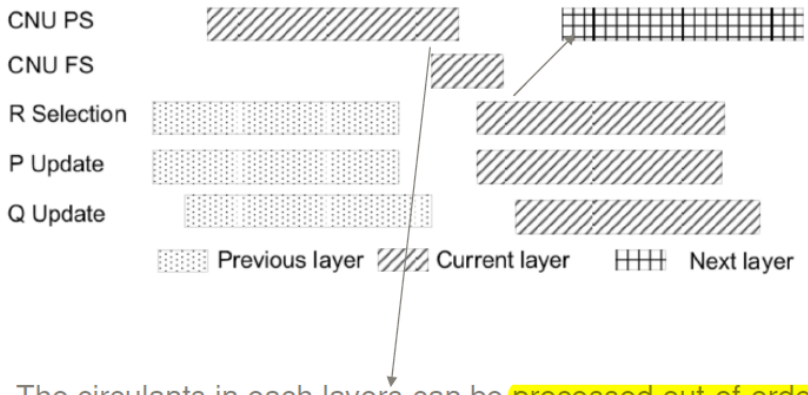


Supports out-of-order processing for PS processing

Out-of-order processing for Rnew

Layer reordering

Out-of-order processing for PS processing



The circulants in each layers can be processed out-of-order

Out-of-order layer processing for R Selection

Rate 2/3 A code:

3	0	-1	-1	2	0	-1	3	7	-1	1	1	-1	-1	-1	-1	1	0	-1	-1	-1	-1	-1	-1
-1	-1	1	-1	36	-1	-1	34	10	-1	-1	18	2	-1	3	0	-1	0	0	-1	-1	-1	-1	-1
-1	-1	12	2	-1	15	-1	40	-1	3	-1	15	-1	2	13	-1	-1	-1	0	0	-1	-1	-1	-1
-1	-1	19	24	-1	3	0	-1	6	-1	17	-1	-1	-1	8	39	-1	-1	-1	0	0	-1	-1	-1
20	-1	6	-1	-1	10	29	-1	-1	28	-1	14	-1	38	-1	-1	0	-1	-1	-1	0	0	-1	-1
-1	-1	10	-1	28	20	-1	-1	8	-1	36	-1	9	-1	21	45	-1	-1	-1	-1	-1	0	0	-1
35	25	-1	37	-1	21	-1	-1	5	-1	-1	0	-1	4	20	-1	-1	-1	-1	-1	-1	-1	0	0
-1	6	6	-1	-1	-1	4	-1	14	30	-1	3	36	-1	14	-1	1	-1	-1	-1	-1	-1	-1	0

○ PS processing □ R selection

R selection is out-of-order so that it can feed the data required for the PS processing of the second layer.

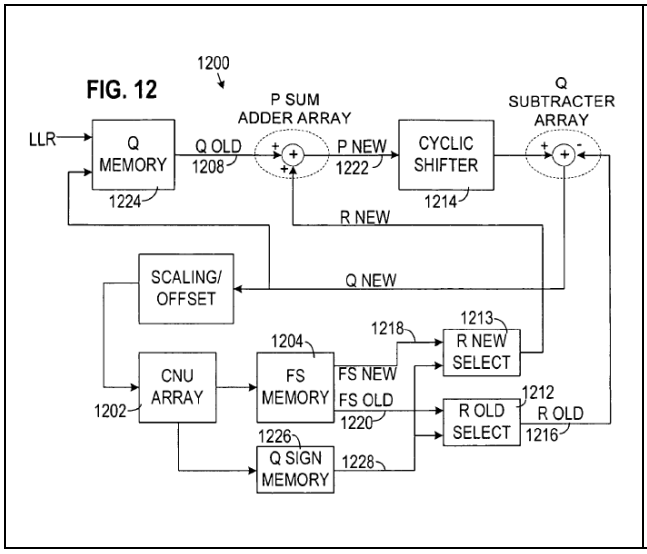
So here we decoupled the execution of R new messages with the execution of CNU processing.

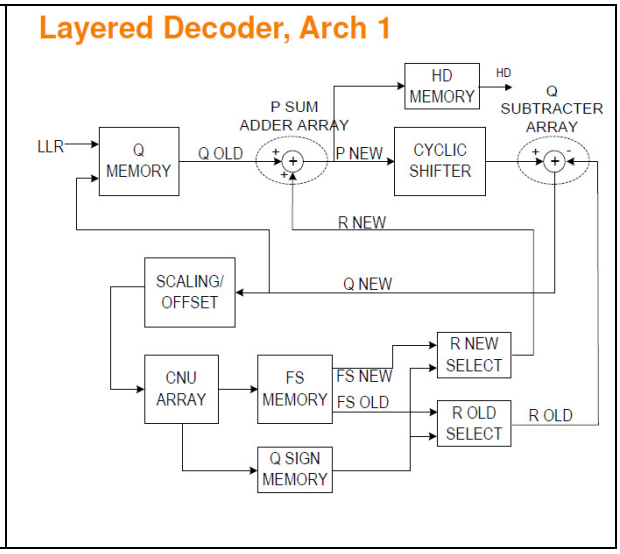
Here we execute the instruction/computation at precise moment when the result is needed!!!

LSI Confidential Internal Use Only 10 LSI

100. The layered decoder architecture of the Accused Products is identical in relevant respects to what is set forth in the '023 patent.

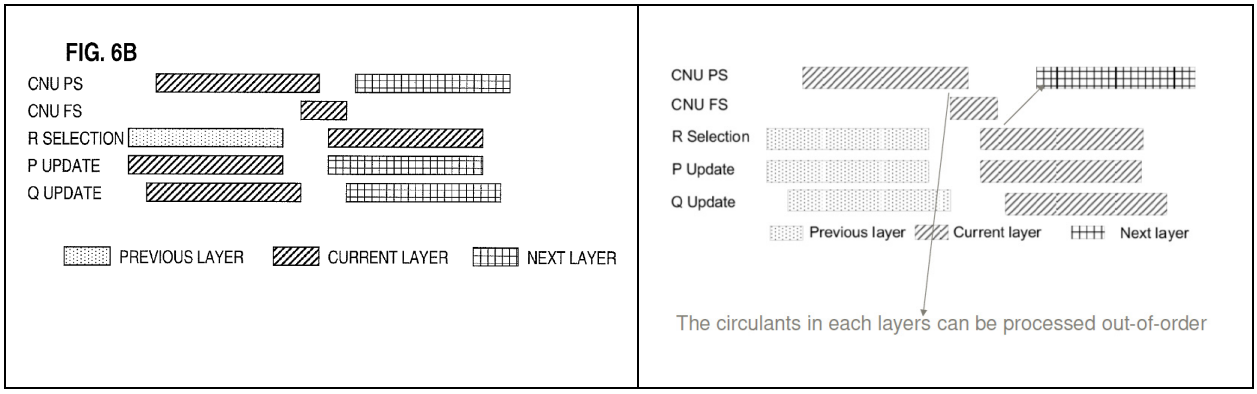
'023 Patent at FIG. 12 **Layered Decoder Presentation at 4**





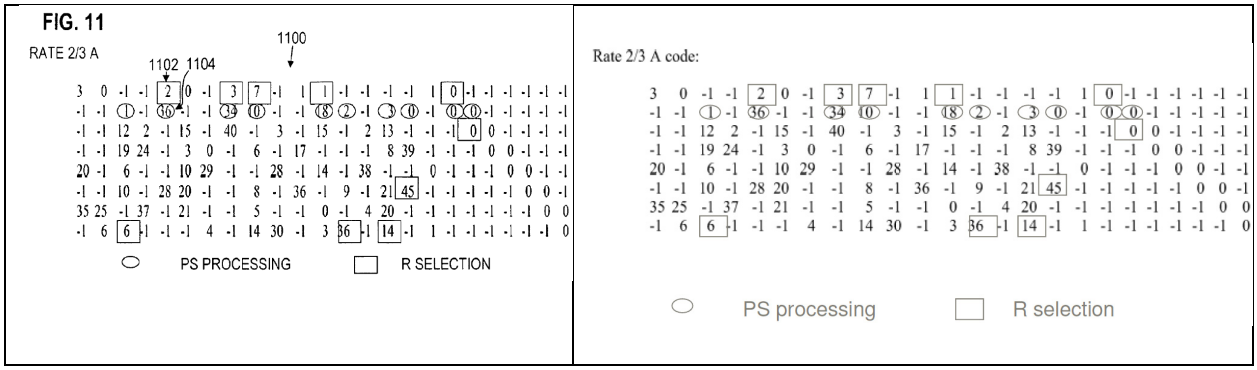
101. The pipeline architecture of the Accused Products is similar to what is set forth in the ’023 patent.

’023 Patent at FIG. 6B | **Layered Decoder Presentation at 8**

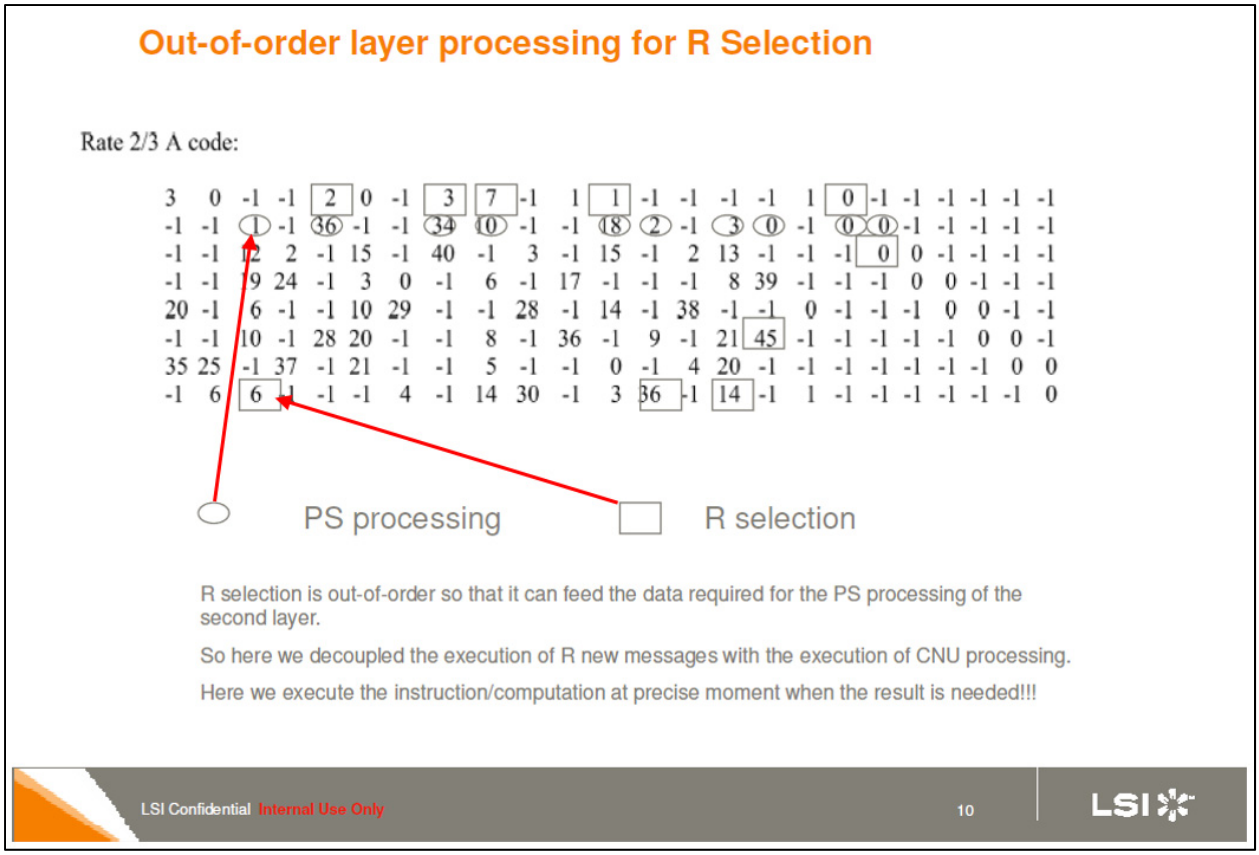


102. The exemplary Rate 2/3 A code of the Accused Products is identical to what is set forth in the ’023 patent.

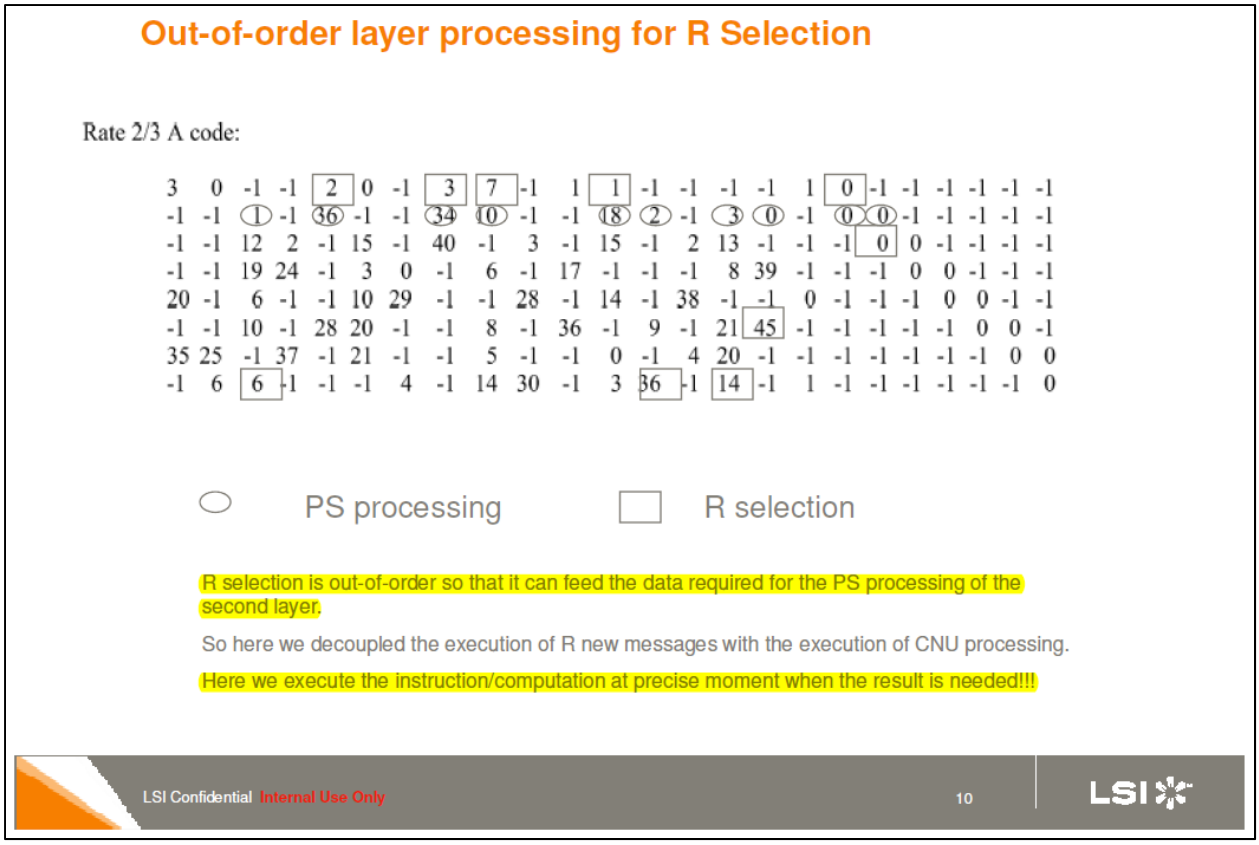
’023 Patent at FIG. 11 | **Layered Decoder Presentation at 10**



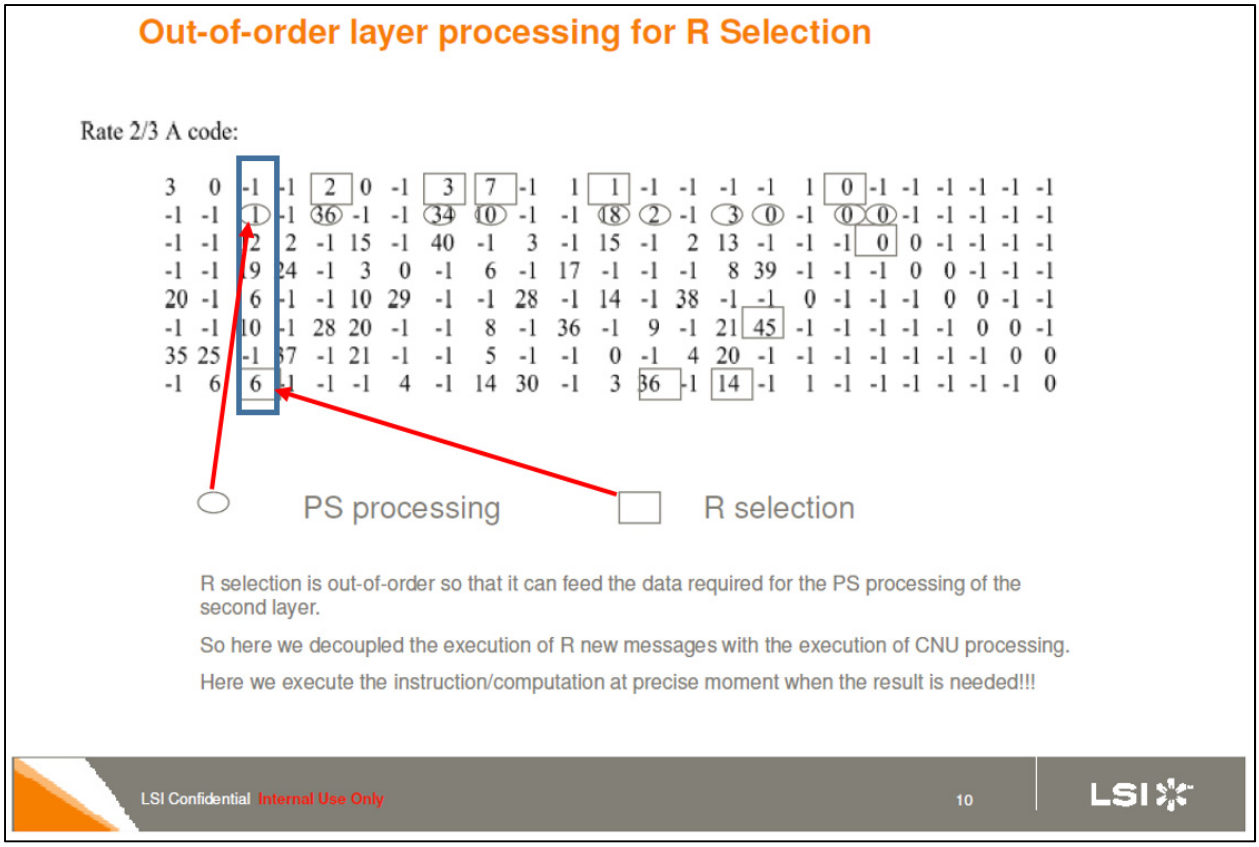
103. The Accused Products schedule computation of R messages for a first non-zero block and computation of P messages and Q messages for a second non-zero block. For example, the Layered Decoder Presentation discloses that the computation of the R messages (“R SELECTION”) are for a first non-zero block and the computation of the P messages and the Q messages are for a second non-zero block.



104. The Accused Products schedule computations such that R messages for the first non-zero block are generated while processing the second non-zero block, based on a determination of need for the R messages for the computation of P and Q messages for the second non-zero block. For example, the Layered Decoder Presentation discloses that the R selection is out-of-order so that it can feed the data required for the P and Q message computation of the second layer.



105. The Accused Products include wherein the first non-zero block and the second non-zero block are in a same column of the matrix. For example, the Layered Decoder Presentation discloses a matrix wherein the first non-zero block and the second non-zero block are in a same column.



106. Claim 18 of the '023 patent recites as follows:

> 18. A method for decoding a low density parity check code, comprising:
> processing blocks of a low density parity check ("LDPC") matrix out of order; and
> scheduling computation of R messages for a first non-zero block and computation of P messages and Q messages for a second non-zero block such that R messages for the first non-zero block are generated while processing the second non-zero block based on a determination of need for the R messages for the computation of P and Q messages for the second non-zero block;
> wherein the first non-zero block and the second non-zero block are in a same column of the matrix.

107. On information and belief, the Accused Products satisfy each and every limitation of Claim 18. The Accused Products decode a low density parity check code. *See* ¶ 91, *supra*.

108. The Accused Products process blocks of a LDPC matrix out of order. *See* ¶¶ 96, 99, *supra*.

109. The Accused Products schedule computation of R messages for a first non-zero block and computation of P messages and Q messages for a second non-zero block. *See* ¶¶ 96, 103, *supra*.

110. The Accused Products schedule computations such that R messages for the first non-zero block are generated while processing the second non-zero block based on a determination of need for the R messages for the computation of P and Q messages for the second non-zero block. *See* ¶¶ 96, 103-04, *supra*.

111. The Accused Products schedule computations wherein the first non-zero block and the second non-zero block are in a same column of the matrix. *See* ¶ 96, 105, *supra*.

112. In view of the foregoing, the Accused Products directly infringe at least Claims 1-30 of the '023 patent at least through Defendant's and/or Broadcom Predecessor Entities' sale, offer for sale, importation, use, and/or testing of the Accused Products.

113. On information and belief, Defendant and/or the Broadcom Predecessor Entities have taken active steps to induce infringement by others of at least Claims 1-30 of the '023 patent in violation of 35 U.S.C. §271(b), including, for example, by (a) inducing manufacturers to practice the claimed inventions when testing the Accused Products, and (b) inducing end users to practice the claimed inventions when using the Accused Products. Such active steps include, but are not limited to, selling Accused Products with the knowledge and intent that the Accused Products will be operated by such manufacturers and their customers in accordance with the claimed inventions.

114. On information and belief, Defendant and/or the Broadcom Predecessor Entities have known or should have known that such activities induce others to directly infringe one or more of at least Claims 1-30 of the '023 patent. For example, Defendant and/or the Broadcom

Predecessor Entities should have known that their actions induced others to directly infringe as of the date it became aware of the issuance of the '023 patent on or about April 9, 2013, and in any event no later than the date it was advised of the issuance of the '023 patent by Dr. Gunnam on January 31, 2014. Defendant and/or the Broadcom Predecessor Entities were further informed that the technology in the Accused Products infringed the '023 patent, and Defendant and/or the Broadcom Predecessor Entities have knowingly and purposefully continued to exploit the patented technology, despite knowing that it was covered by the '023 patent.

115. On information and belief, Defendant and/or the Broadcom Predecessor Entities have contributed to the infringement of at least Claims 1-30 of the '023 patent by others, including consumer/end-user use of the Accused Products, in violation of 35 U.S.C. § 271(c). Acts by Defendant and/or the Broadcom Predecessor Entities that have contributed to the infringement of others include, but are not limited to, the sale, offer for sale, and/or import by Defendant of the Accused Products. Such Accused Products are especially made for or adapted for use to infringe, and are not a staple article of commerce and are not suitable for substantial non-infringing use. The Accused Products are apparatuses for use in practicing the inventions patented in Claims 1-30 of the '023 patent, and are at least a material part of those claimed inventions, for example, as described above with respect to Claim 18. On information and belief, the steps recited in Claim 18, for example, are performed by the Accused Products.

116. As also described above, Defendant and/or the Broadcom Predecessor Entities have, on information and belief, been on notice of the '023 patent since it issued on April 9, 2013 and in any event were on notice as of no later than January 31, 2014.

117. In addition, Defendant has been on notice since the filing and/or service of this Complaint. Defendant has further been aware that use of the Accused Products necessarily practice the inventions in Claims 1-30 of the '023 patent.

118. The Accused Products are especially made for or adapted for use to infringe, and are not a staple article of commerce, and are not suitable for substantial non-infringing use. By way of example, the use of the LDPC decoders included in the Accused Products is necessary to use the accused products for their intended purpose (decoding data from a hard disk drive, solid state drive, or wireless digital transmission), and the LDPC decoders necessarily practice the claimed inventions when they decode data. Accordingly, the Accused Products do not have a substantial use that does not entail practicing the claimed inventions. On information and belief, the Accused Products cannot be used but to infringe the '023 patent.

119. Despite Defendant's and/or the Broadcom Predecessor Entities' knowledge and notice of the '023 patent and its ongoing infringement, Defendant and/or the Broadcom Predecessor Entities have continued to manufacture, use, sell, offer for sale, and/or import the Accused Products in a manner that willfully infringes the '023 patent, and on information and belief, continue to sell and/or offer for sale the Accused Products to the United States market. On information and belief, nearly all of Dr. Gunnam's work, *inter alia*, at LSI was centered on the TAMUS' '320 provisional application. On information and belief, LSI recognized its competitive disadvantage from not having acquired the rights to the Patents-in-Suit for itself, and embarked on a course of action where it filed and prosecuted at least 48 to 68 patents, based on Dr. Gunnam's work concerning the TAMUS '320 provisional application.

See https://www.google.com/search?tbm=pts&ei=lR4QXM-pHrm40PEP_s6YwAE&q=Ser.+No.+12%2F113%2C729+filed+on+May+1%2C+2008&oq=Ser.+No.+12%2F113%2C729+filed+on+May+1%2C+2008&gs_l=psy-ab.3...95601.99862.0.100208.3.3.0.0.0.0.128.258.2j1.3.0....0...1c.1.64.psy-ab..0.0.0....0.OmH6jRmYHJo; *see also* https://www.google.com/search?tbm=pts&ei=jB4QXODdHdC60PEP0qC4-A4&q=Ser.+No.+12%2F113%2C755+filed+on+May+1%2C+2008&oq=Ser.+No.+12%2F113%2C755+filed+on+May+1%2C+2008&gs_l=psy-ab.3...7529.7728.0.8111.2.2.0.0.0.0.81.149.2.2.0....0...1c.1.64.psy-ab..0.0.0....0.UBEXLdczJgA. On information and belief, LSI filed and prosecuted these patents despite Dr. Gunnam's repeated requests to LSI management for LSI to obtain a license for the TAMUS intellectual property. Defendant and/or the Broadcom Predecessor Entities' infringement of the '023 patent has thus been willful, as set forth above. Defendant and/or the Broadcom Predecessor Entities lacked a justifiable belief that they did not infringe the '023 patent, or that the '023 patent is invalid or unenforceable, and have acted recklessly in their infringing activity, justifying an increase in the damages to be awarded to Plaintiff up to three times the amount found or assessed, in accordance with 35 U.S.C. § 284.

120. On information and belief, Defendant and/or the Broadcom Predecessor Entities have had actual or constructive knowledge of the '023 patent since at least April 9, 2013, and in any event no later than January 31, 2014.

121. Defendant further has knowledge of the '023 patent at least as early as the filing and/or service of this Complaint. Defendant knows or should know as of the date of filing and/or

service of the Complaint that its actions induced others to directly infringe the '023 patent and contributed to infringement of the '023 patent.

122. This case is rendered an exceptional case at least in light of Defendant's and/or the Broadcom Predecessor Entities' willful infringement of the '023 patent, justifying an award to Plaintiff of its reasonable attorney fees, in accordance with 35 U.S.C. § 285.

123. Plaintiff has no adequate remedy at law for Defendant's acts of infringement. As a direct and proximate result of Defendant's acts of infringement, Plaintiff has suffered and continues to suffer damages and irreparable harm. Unless Defendant's acts of infringement are enjoined by this Court, Plaintiff will continue to be damaged and irreparably harmed.

124. Defendant's and/or the Broadcom Predecessor Entities' infringement of the '023 patent has damaged and continues to damage Plaintiff in an amount yet to be determined, of at least a reasonable royalty and/or lost profits that Plaintiff would have made but for Defendant's infringement acts.

COUNT II
(Infringement under 35 U.S.C. § 271 of U.S. Patent No. 8,555,140)

125. Plaintiff repeats and re-alleges the paragraphs above as if fully set forth herein.

126. The '140 patent is valid, enforceable, and was duly issued on October 8, 2013 in full compliance with Title 35 of the United States Code.

127. On information and belief, in violation of 35 U.S.C. § 271, Defendant and/or the Broadcom Predecessor Entities have infringed, contributed to the infringement of, and/or induced others to infringe the '140 patent, either literally or under the doctrine of equivalents, by, among other things, making, using, offering for sale, selling, and/or importing into the United

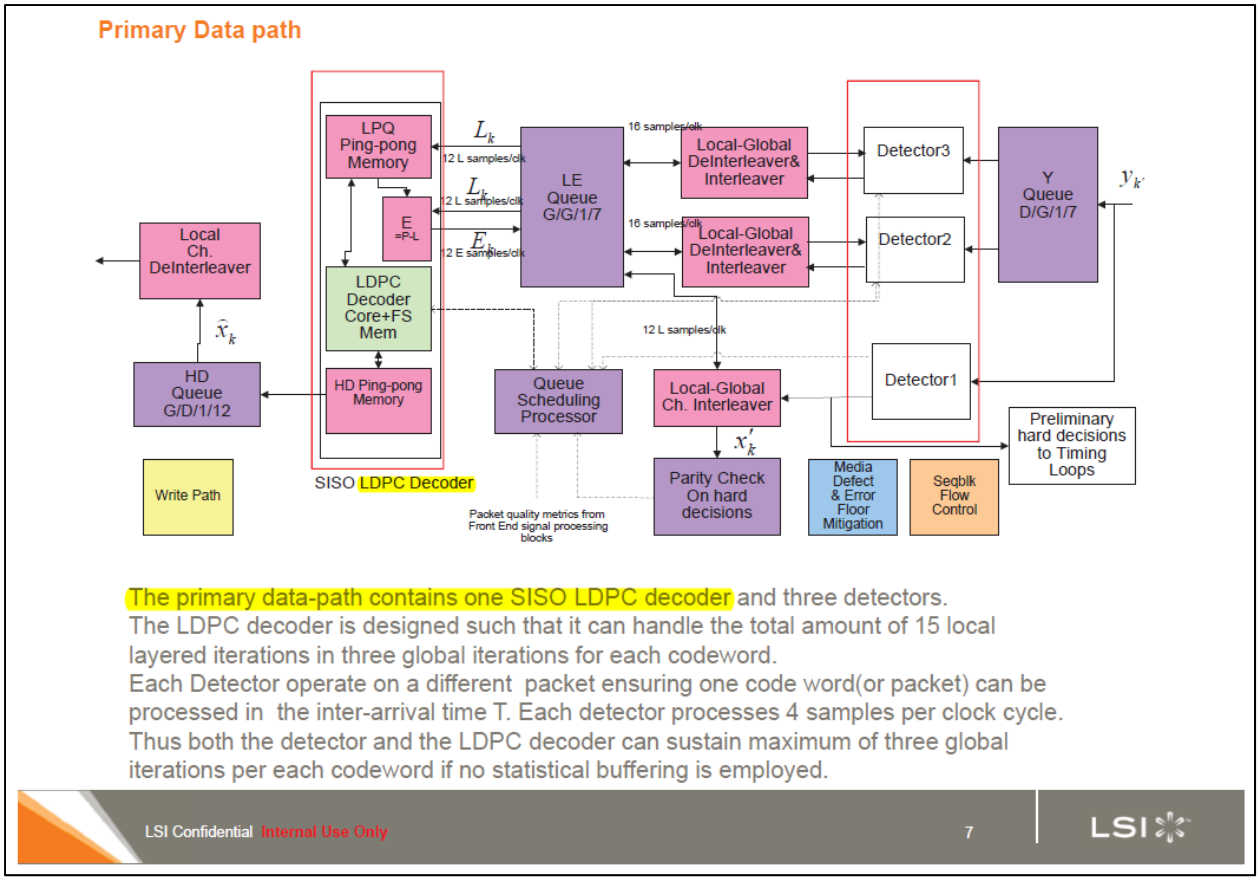
States unlicensed systems and/or products in a manner that infringes at least Claims 7-12 and 18-22 of the '140 patent.

128. On information and belief, Defendant and/or the Broadcom Predecessor Entities have directly infringed the '140 patent, for example, by making, using, selling, offering to sell, and/or importing into the United States the Accused Products, which meet each and every limitation of at least Claim 7 of the '140 patent, in violation of Plaintiff's patent rights and without Plaintiff's license or authority. Non-limiting examples of such infringement are provided below, based on the limited information currently available to Plaintiff.

129. Claim 7 of the '140 patent recites as follows:

> 7. A method for decoding a low density parity check (LDPC) code, comprising:
> processing blocks of an LDPC matrix in a first sequence; computing R messages for the blocks in a second sequence that is different from the first sequence; specifying, via the first sequence, a first set of blocks of a given layer to be processed at a given time and a second set of blocks of the given layer to be processed after the first set of blocks; wherein the first set specifies only blocks of the given layer that are not dependent on a result of a previously processed layer and the second set specifies blocks of the given layer that are dependent on a result of the previously processed layer.

130. On information and belief, the Accused Products satisfy each and every limitation of Claim 7. The Accused Products decode an LDPC code. For example, the McLaren Architecture Presentation references the LDPC decoder.



131. The Accused Products process blocks of an LDPC matrix in a first sequence and compute R messages for the blocks in a second sequence that is different from the first sequence. For example, the Layered Decoder Presentation indicates that the Accused Products process blocks of an LDPC matrix in a first sequence and compute R messages for the blocks in a different sequence.

Out-of-order layer processing for R Selection

Rate 2/3 A code:

3	0	-1	-1	2	0	-1	3	7	-1	1	1	-1	-1	-1	-1	1	0	-1	-1	-1	-1	-1	-1
-1	-1	1	-1	36	-1	-1	34	10	-1	-1	18	2	-1	3	0	-1	0	0	-1	-1	-1	-1	-1
-1	-1	12	2	-1	15	-1	40	-1	3	-1	15	-1	2	13	-1	-1	-1	0	0	-1	-1	-1	-1
-1	-1	19	24	-1	3	0	-1	6	-1	17	-1	-1	-1	8	39	-1	-1	-1	0	0	-1	-1	-1
20	-1	6	-1	-1	10	29	-1	-1	28	-1	14	-1	38	-1	-1	0	-1	-1	-1	0	0	-1	-1
-1	-1	10	-1	28	20	-1	-1	8	-1	36	-1	9	-1	21	45	-1	-1	-1	-1	-1	0	0	-1
35	25	-1	37	-1	21	-1	-1	5	-1	-1	0	-1	4	20	-1	-1	-1	-1	-1	-1	-1	0	0
-1	6	6	-1	-1	-1	4	-1	14	30	-1	3	36	-1	14	-1	1	-1	-1	-1	-1	-1	-1	0

PS processing R selection

R selection is out-of-order so that it can feed the data required for the PS processing of the second layer.

So here we decoupled the execution of R new messages with the execution of CNU processing.

Here we execute the instruction/computation at precise moment when the result is needed!!!

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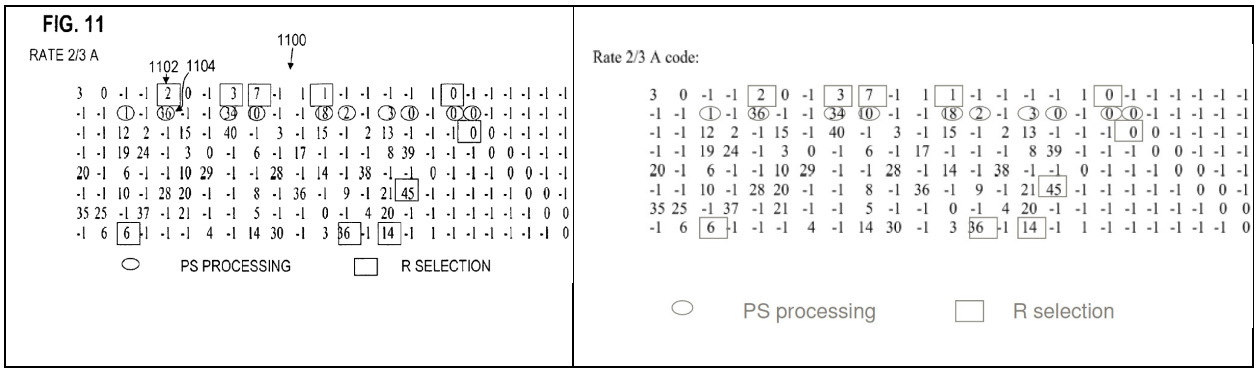
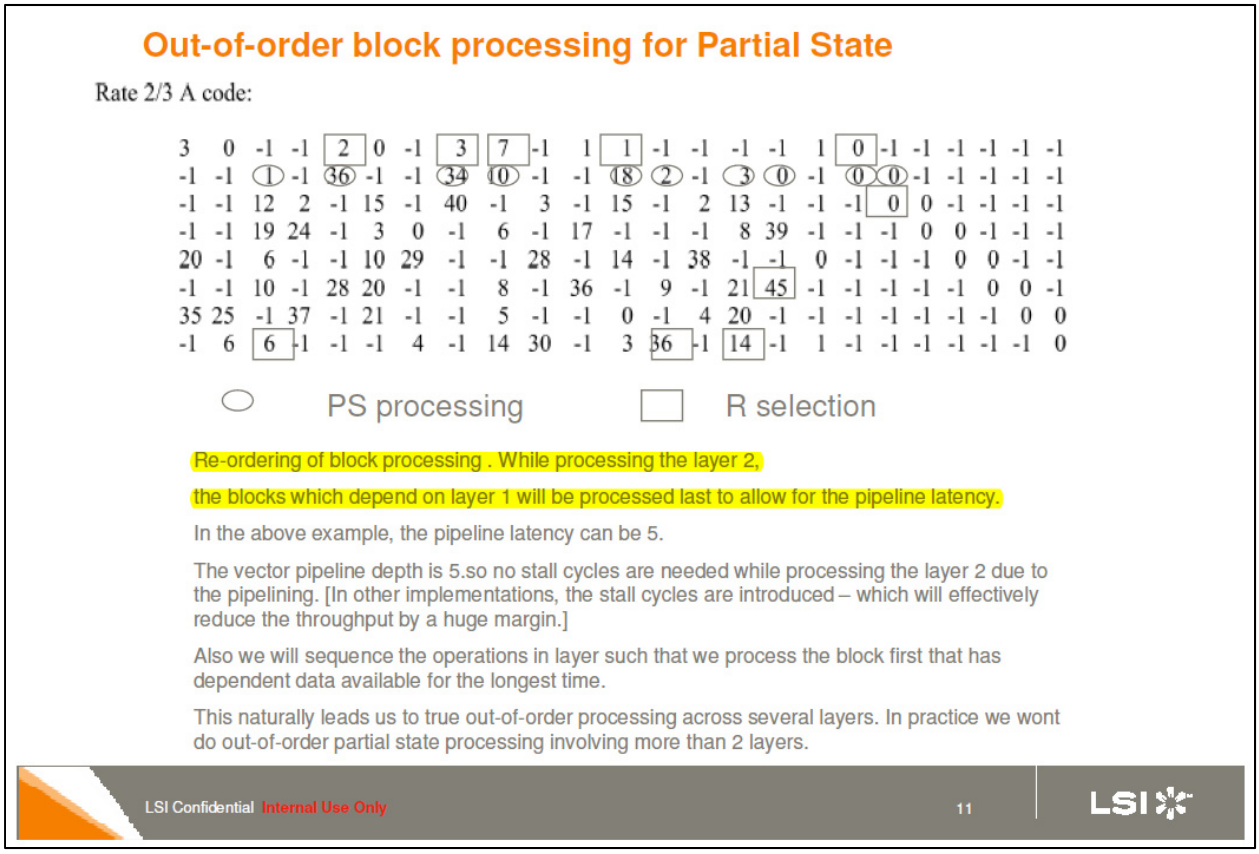
132. The exemplary Rate 2/3 A code of the Accused Products is identical to what is set forth in the '140 patent.

'140 Patent at FIG. 11 **Layered Decoder Presentation at 10**



133. The Accused Products specify, via the first sequence, a first set of blocks of a given layer to be processed at a given time and a second set of blocks of the given layer to be processed after the first set of blocks, wherein the first set specifies only blocks of the given layer that are not dependent on a result of a previously processed layer and the second set specifies blocks of the given layer that are dependent on a result of the previously processed layer. For example, the Layered Decoder Presentation discloses that while processing the second layer, the blocks which depend on layer 1 will be processed last.



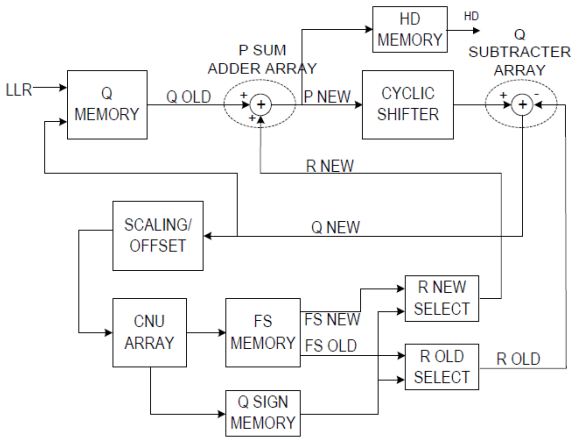
134. Claim 18 of the ’140 patent recites as follows:

> 18. A method for decoding a low density parity check (LDPC) code, comprising:
> processing blocks of an LDPC matrix out of order; and
> processing each block of the matrix in processing substeps comprising:
> an R new update substep that produces an R new message for a block of a different layer of the matrix from a layer containing a block currently being processed;
> an R old update substep that selects an R old message for a layer of the matrix currently being processed;
> a P message substep that generates updated P messages; and
> a Q message substep that computes variable node messages (Q messages);
> permuting a P message, wherein the permuting comprises permuting the P message by the difference of the permutation of a block currently being processed and the permutation of a block previously processed; wherein the block currently being processed and the block previously processed are in a same block column.

135. On information and belief, the Accused Products satisfy each and every limitation of Claim 18. The Accused Products decode an LDPC code. *See* ¶ 132, 91, *supra*.

136. The Accused Products process blocks of an LDPC matrix out of order. For example, the Layered Decoder Presentation references out of order processing and includes many figures taken directly from the ’140 patent.

Layered Decoder, Arch 1

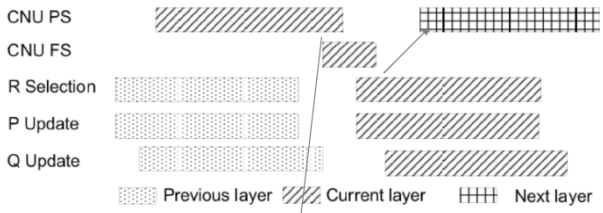


Supports out-of-order processing for PS processing

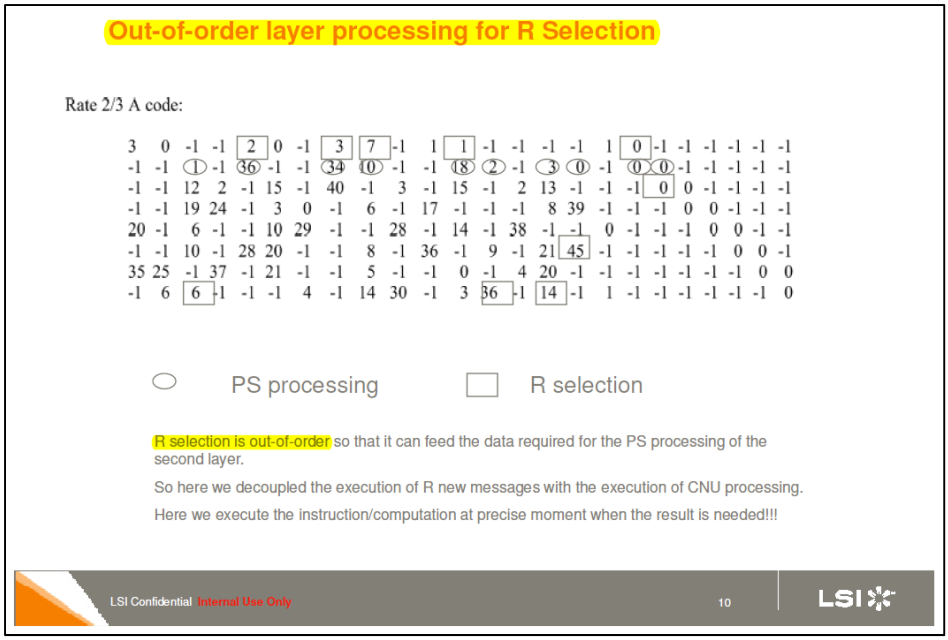
Out-of-order processing for Rnew

Layer reordering

Out-of-order processing for PS processing

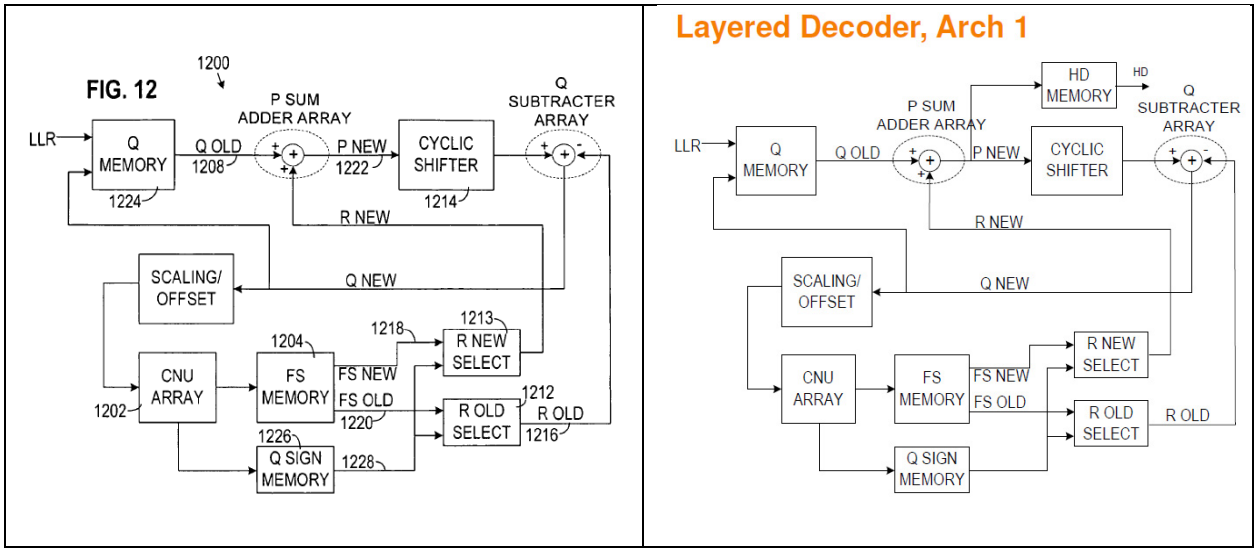


The circulants in each layers can be processed out-of-order



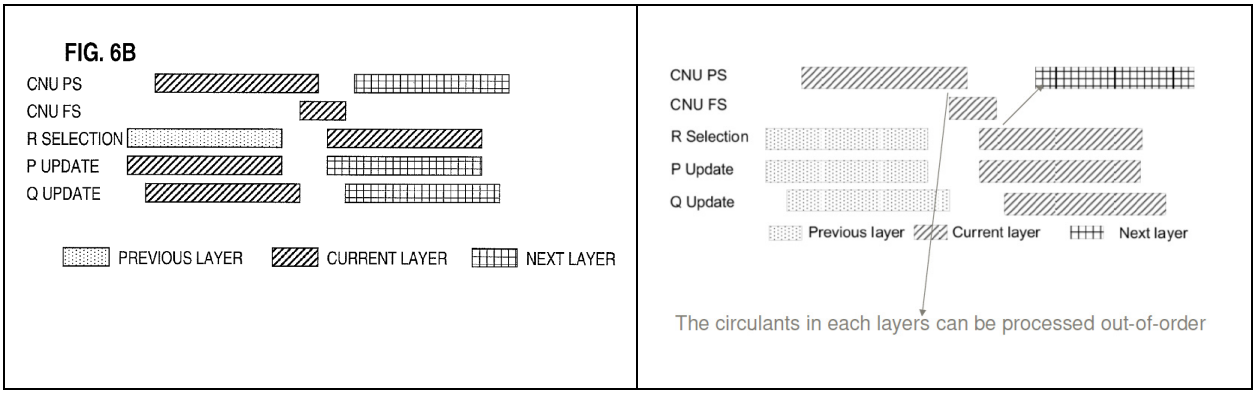
137. The layered decoder architecture of the Accused Products is identical to what is set forth in the '140 patent.

'140 Patent at FIG. 12 | **Layered Decoder Presentation at 4**

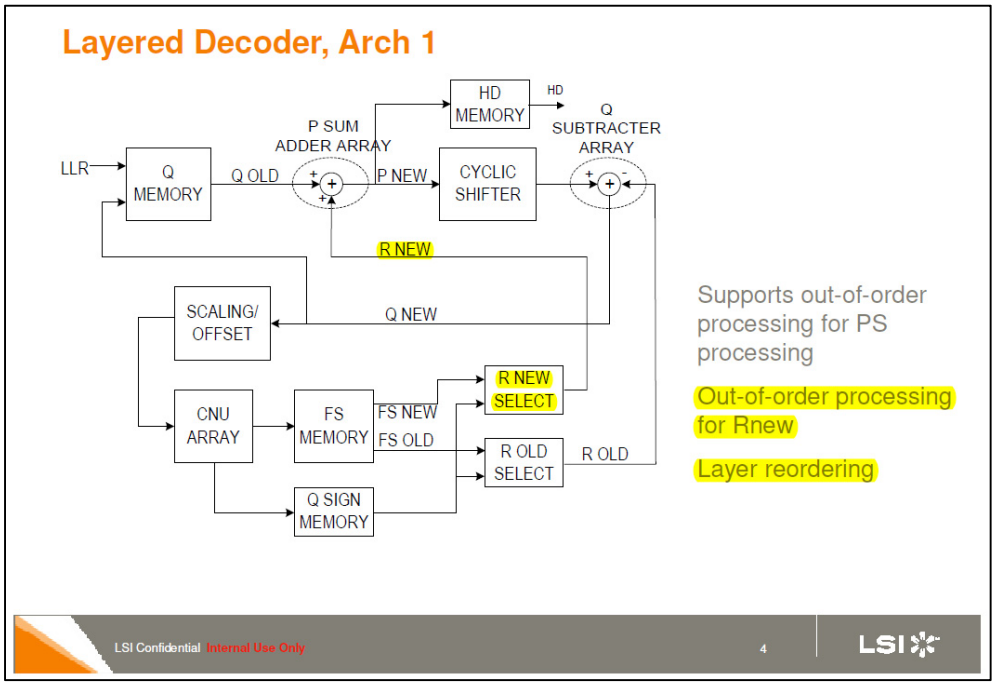


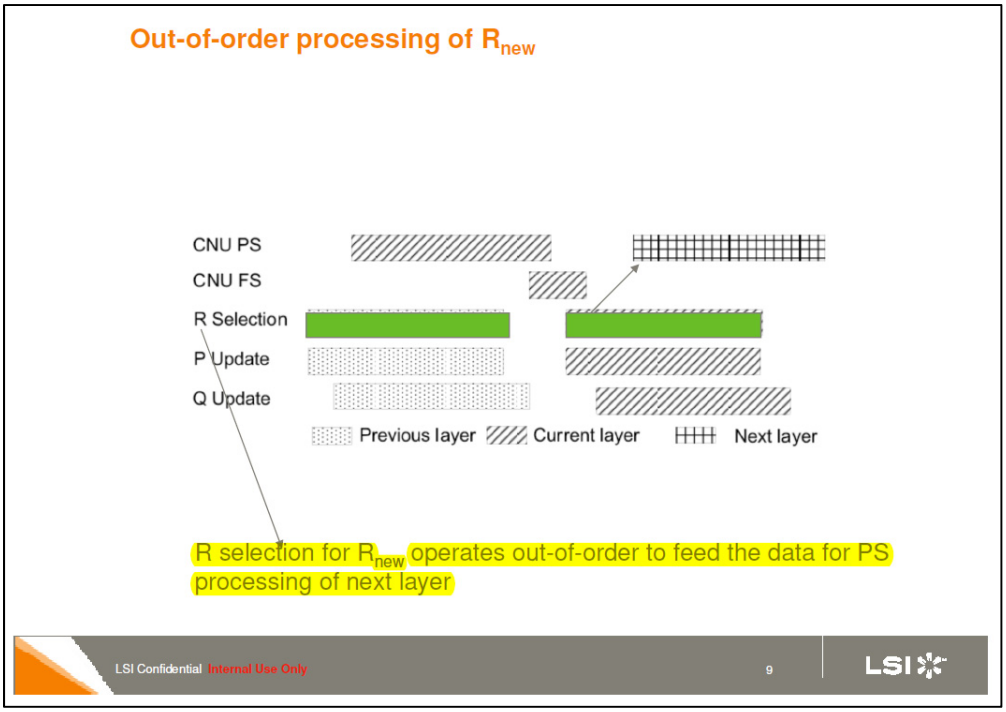
138. The pipeline architecture of the Accused Products is similar to what is set forth in the '140 patent.

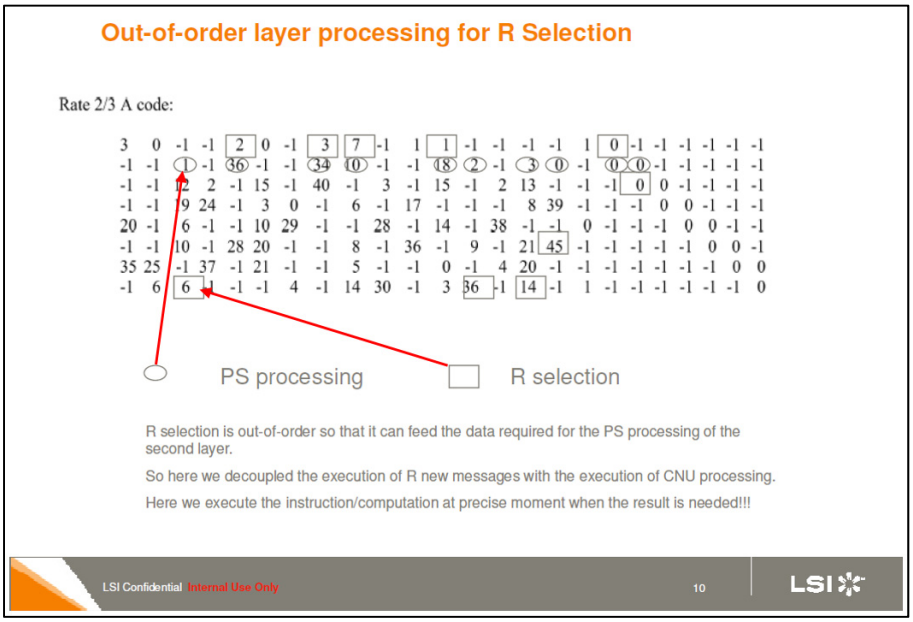
'140 Patent at FIG. 6B | **Layered Decoder Presentation at 8**



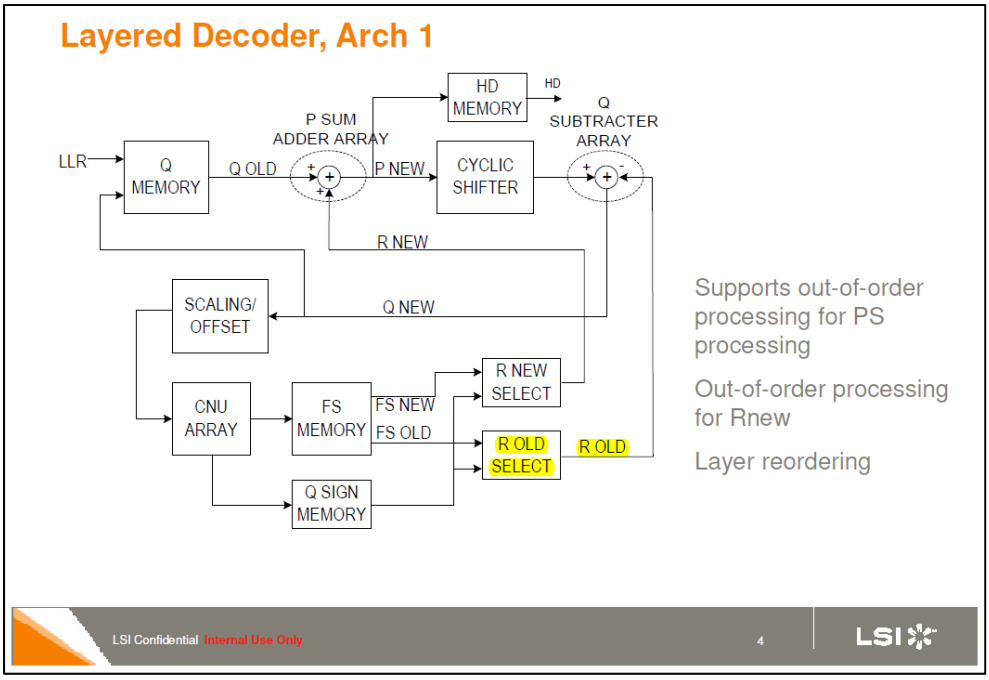
139. The Accused Products process each block of the matrix in processing substeps comprising an R new update substep that produces an R new message for a block of a different layer of the matrix from a layer containing a block currently being processed. For example, the Layered Decoder Presentation discloses an R NEW SELECT unit that produces an R new message for a block of a different layer of the matrix from a layer containing a block currently being processed.



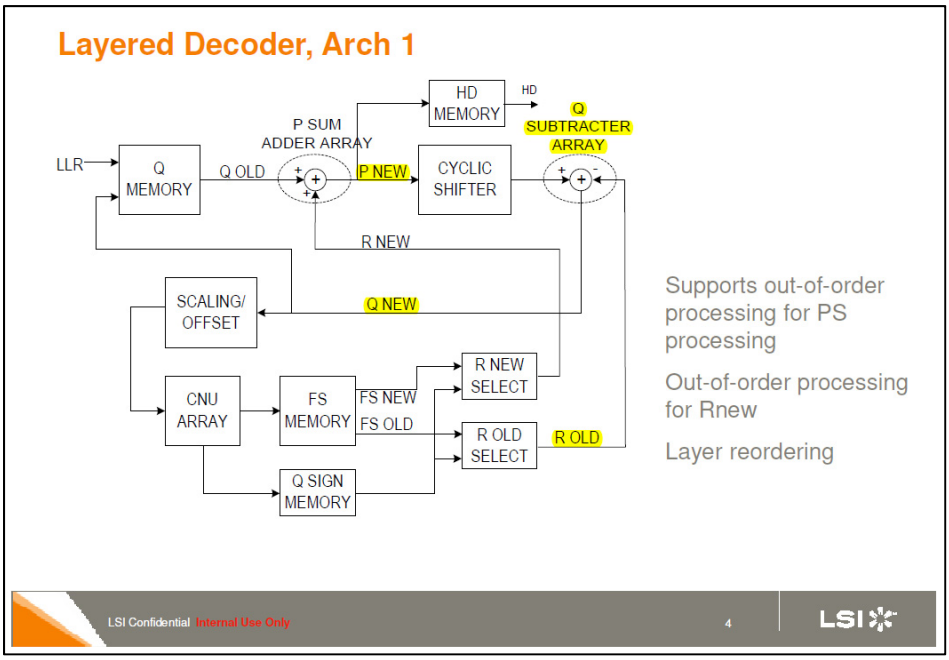




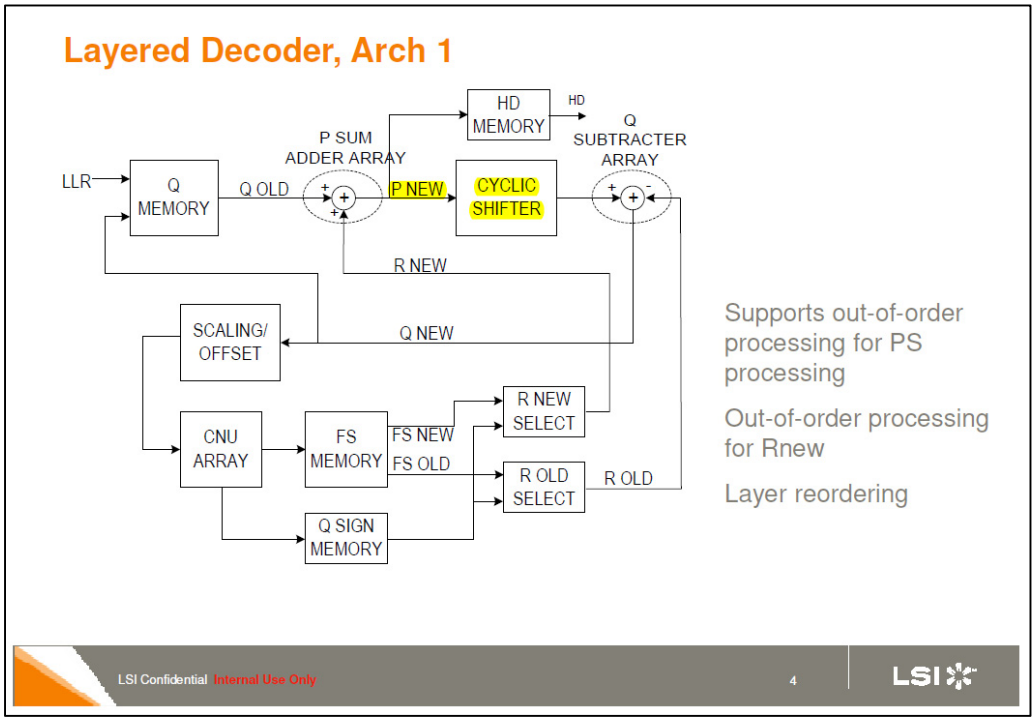
140. The Accused Products process each block of the matrix in processing substeps comprising an R old update substep that selects an R old message for a layer of the matrix currently being processed. For example, the Layered Decoder Presentation discloses an R OLD SELECT unit that selects an R old message for a layer of the matrix currently being processed.



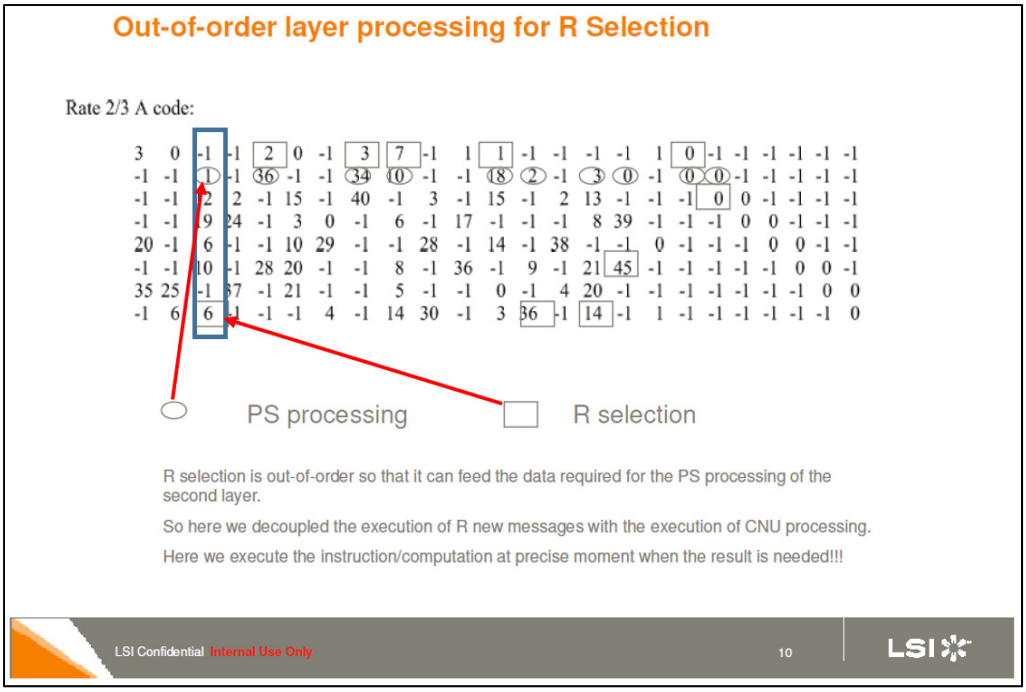
141. The Accused Products process each block of the matrix in processing substeps comprising a Q message substep that computes variable node messages (Q messages). For example, the Layered Decoder Presentation discloses a Q SUBTRACTER ARRAY that computes variable node messages (Q messages).



142. The Accused Products permute a P message, wherein the permuting comprises permuting the P message by the difference of the permutation of a block currently being processed and the permutation of a block previously processed. For example, the Layered Decoder Presentation discloses the presence of CYCLIC SHIFTER configured to permute a P message by the difference of the permutation of a block currently being processed and the permutation of a block previously processed.



143. The Accused Products permute a P message wherein the block currently being processed and the block previously processed are in a same block column. For example, the Layered Decoder Presentation discloses that the computation of the R messages ("R SELECTION") for a first non-zero block are generated while processing the second non-zero block ("PS PROCESSING"), and these two blocks are in a same block column of an LDPC matrix.



144. In view of the foregoing, Defendant and/or the Broadcom Predecessor Entities have directly infringed at least Claims 7-12 and 18-22 of the '140 patent through their internal testing, use, and operation of the Accused Products.

145. On information and belief, Defendant and/or the Broadcom Predecessor Entities have had actual or constructive knowledge of the '140 patent since at least January 22, 2013, as noted above.

146. Defendant further has knowledge of the '140 patent at least as early as the filing and/or service of this Complaint.

147. On information and belief, Defendant and/or the Broadcom Predecessor Entities have taken active steps to induce infringement by others of at least Claims 7-12 and 18-22 of the '140 patent in violation of 35 U.S.C. §271(b), including, for example, by (a) inducing manufacturers to perform the claimed inventions when testing the Accused Products, and (b) inducing end users to perform the claimed inventions when using the Accused Products. Such

active steps include, but are not limited to, selling Accused Products with the knowledge and intent that the Accused Products will be operated by such manufacturers and their customers in accordance with the claimed inventions.

148. On information and belief, Defendant and/or the Broadcom Predecessor Entities have known or should have known that such activities induce others to directly infringe one or more of at least claims 7-12 and 18-22 of the '140 patent. For example, Defendant and/or the Broadcom Predecessor Entities should have known that their actions induced others to directly infringe as of the date it became aware of the issuance of the '140 patent on or about October 8, 2013, and in any event no later than the date they were advised of the issuance of the '140 patent by Dr. Gunnam on January 31, 2014. Defendant and/or the Broadcom Predecessor Entities were further informed that the technology in the Accused Products infringed the '140 patent, and Defendant and/or the Broadcom Predecessor Entities have knowingly and purposefully continued to exploit the patented technology despite knowing that it was covered by the '140 patent.

149. On information and belief, Defendant and/or the Broadcom Predecessor Entities have contributed to the infringement of at least Claims 7-12 and 18-22 of the '140 patent by others, including consumer/end-user use of the Accused Products, in violation of 35 U.S.C. § 271(c). Acts by Defendant and/or the Broadcom Predecessor Entities that contribute to the infringement of others include, but are not limited to, the sale, offer for sale, and/or import by Defendant and/or the Broadcom Predecessor Entities of the Accused Products. Such Accused Products are especially made for or adapted for use to infringe, and are not a staple article of commerce and are not suitable for substantial non-infringing use. The Accused Products are apparatuses for use in practicing the inventions patented in Claims 7-12 and 18-22 of the '140

patent, and are at least a material part of those claimed inventions, for example, as described above with respect to claims 7 and 18. On information and belief, the steps recited in Claims 7 and 18, for example, are performed by the Accused Products. As also described above, Defendant and/or the Broadcom Predecessor Entities have, on information and belief, been on notice of the '140 patent since it issued on October 8, 2013, and in any event no later than January 31, 2014.

150. In addition, Defendant has been aware of the '140 patent since filing and/or service of this Complaint, and Defendant and/or the Broadcom Predecessor Entities have further been aware that use of the Accused Products necessarily practice the inventions in Claims 7-12 and 18-22 of the '140 patent.

151. The Accused Products are especially made for or adapted for use to infringe, and are not a staple article of commerce and are not suitable for substantial non-infringing use. By way of example, the use of the LDPC decoders included in the Accused Products is necessary to use the accused products for their intended purpose (decoding data from a hard disk drive, solid state drive, or wireless digital transmission), and the LDPC decoders necessarily perform the claimed inventions when they decode data. Accordingly, the Accused Products do not have a substantial use that does not entail practicing the claimed inventions. On information and belief, the Accused Products cannot be used but to infringe the '140 patent.

152. Despite Defendant's knowledge and notice of the '140 patent and its ongoing infringement, Defendant continues to test or use the Accused Products in a manner that willfully infringes the '140 patent, and on information and belief continues to sell and/or offer for sale the Accused Products to the United States market for customers / end users to infringe. On information and belief, nearly all of Dr. Gunnam's work, *inter alia*, at LSI was centered on the

TAMUS' '320 provisional application. On information and belief, LSI recognized its competitive disadvantage from not having acquired the rights to the Patents-in-Suit for itself, and embarked on a course of action where it filed and prosecuted at least 48 to 68 patents, based on Dr. Gunnam's work concerning the TAMUS '320 provisional application. *See* https://www.google.com/search?tbm=pts&ei=lR4QXM-pHrm40PEP_s6YwAE&q=Ser.+No.+12%2F113%2C729+filed+on+May+1%2C+2008&oq=Ser.+No.+12%2F113%2C729+filed+on+May+1%2C+2008&gs_l=psy-ab.3...95601.99862.0.100208.3.3.0.0.0.0.128.258.2j1.3.0....0...1c.1.64.psy-ab..0.0.0....0.OmH6jRmYHJo; *see also* https://www.google.com/search?tbm=pts&ei=jB4QXODdHdC60PEP0qC4-A4&q=Ser.+No.+12%2F113%2C755+filed+on+May+1%2C+2008&oq=Ser.+No.+12%2F113%2C755+filed+on+May+1%2C+2008&gs_l=psy-ab.3...7529.7728.0.8111.2.2.0.0.0.0.81.149.2.2.0....0...1c.1.64.psy-ab..0.0.0....0.UBEXLdczJgA. On information and belief, LSI filed and prosecuted these patents despite Dr. Gunnam's repeated requests to LSI management for LSI to obtain a license for the TAMUS intellectual property. Defendant's infringement of the '140 patent is thus willful, as set forth above. Defendant lacks a justifiable belief that it does not infringe the '140 patent, or that the '140 patent is invalid or unenforceable, and has acted recklessly in its infringing activity, justifying an increase in the damages to be awarded to Plaintiff up to three times the amount found or assessed, in accordance with 35 U.S.C. § 284.

153. This case is rendered an exceptional case at least in light of Defendant's willful infringement of the '140 patent, justifying an award to Plaintiff of its reasonable attorney fees, in accordance with 35 U.S.C. § 285.

154. Plaintiff has no adequate remedy at law for Defendant's acts of infringement. As a direct and proximate result of Defendant's acts of infringement, Plaintiff has suffered and continues to suffer damages and irreparable harm. Unless Defendant's acts of infringement are enjoined by this Court, Plaintiff will continue to be damaged and irreparably harmed.

155. Defendant's and/or the Broadcom Predecessor Entities' infringement of the '140 patent has damaged and continues to damage Plaintiff in an amount yet to be determined, of at least a reasonable royalty and/or lost profits that Plaintiff would have made but for Defendant's infringement acts.

COUNT III
(Infringement under 35 U.S.C. § 271 of U.S. Patent No. 9,112,530)

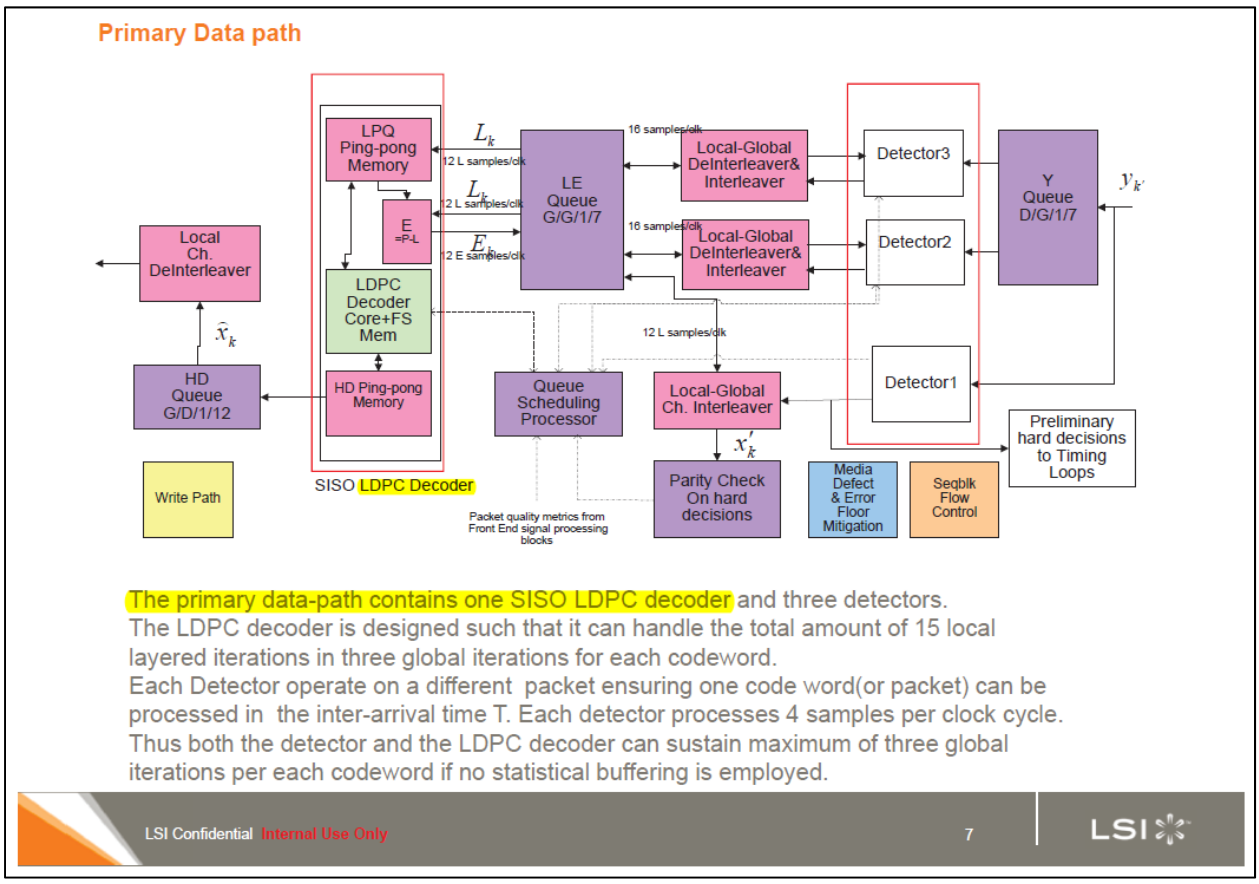
156. Plaintiff repeats and re-alleges the paragraphs above as if fully set forth herein.

157. The '530 patent is valid, enforceable, and was duly issued on August 18, 2015 in full compliance with Title 35 of the United States Code.

158. On information and belief, in violation of 35 U.S.C. § 271, Defendant and/or the Broadcom Predecessor Entities have infringed, contributed to the infringement of, and/or induced others to infringe the '530 patent, either literally or under the doctrine of equivalents, by, among other things, making, using, offering for sale, selling, and/or importing into the United States unlicensed systems and/or products in a manner that infringes at least Claims 13-20, 22-23, and 25-31 of the '530 patent.

159. On information and belief, Defendant and/or the Broadcom Predecessor Entities have directly infringed the '530 patent, for example, by making, using, selling, offering to sell, and/or importing into the United States the Accused Products, which meet each and every limitation of at least Claims 13-20, 22-23, and 25-31 of the '530 patent in violation of Plaintiff's patent rights and without Plaintiff's license or authority. Non-limiting examples of such

infringement are provided below, based on the limited information currently available to



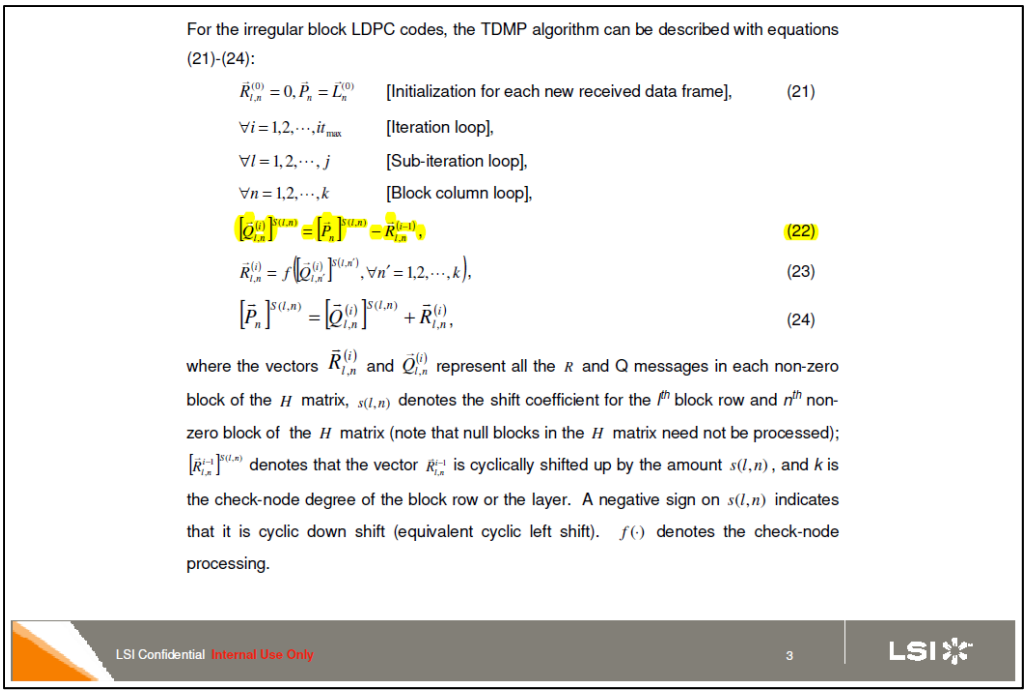
Plaintiff.

160. Claim 13 of the ’530 patent recites as follows:

> 13. A low density parity check (LDPC) code decoder, comprising:
> a Q message generator configured to combine an R message with a P message to produce a Q message;
> logic configured to reduce the magnitude a Q message provided to a check node unit of the decoder; and
> a permuter configured to permute the P message by a difference of permutation of a block currently being processed and permutation of a block previously processed; wherein the block currently being processed and the block previously processed are in a same block column of an LDPC matrix.

161. On information and belief, the Accused Products satisfy each and every limitation of Claim 13. The Accused Products include an LDPC code decoder. For example, the McLaren Architecture Presentation references the LDPC decoder.

162. The Accused Products include a Q message generator configured to combine an R message with a P message to produce a Q message. For example, the Layered Decoder Presentation uses equations and figures taken directly from the '530 patent to disclose the presence of a Q SUBTRACTER ARRAY configured to combine an R message with a P message to produce a Q message.



For the irregular block LDPC codes, the TDMP algorithm can be described with equations (21)-(24):

$\vec{R}_{l,n}^{(0)} = 0, \vec{P}_n = \vec{L}_n^{(0)}$ [Initialization for each new received data frame], (21)

$\forall i = 1,2,\cdots, it_{\max}$ [Iteration loop],

$\forall l = 1,2,\cdots, j$ [Sub-iteration loop],

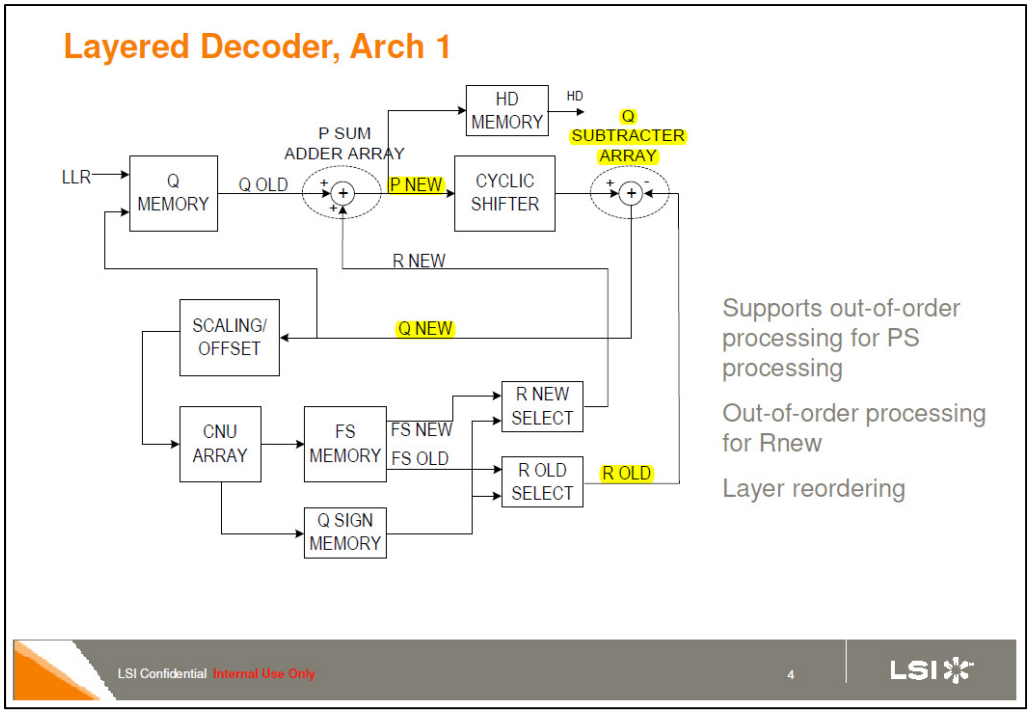
$\forall n = 1,2,\cdots, k$ [Block column loop],

$$\left[\vec{Q}_{l,n}^{(i)}\right]^{S(l,n)} = \left[\vec{P}_n\right]^{S(l,n)} - \vec{R}_{l,n}^{(i-1)}, \quad (22)$$

$$\vec{R}_{l,n}^{(i)} = f\left(\left[\vec{Q}_{l,n'}^{(i)}\right]^{S(l,n')}, \forall n' = 1,2,\cdots,k\right), \quad (23)$$

$$\left[\vec{P}_n\right]^{S(l,n)} = \left[\vec{Q}_{l,n}^{(i)}\right]^{S(l,n)} + \vec{R}_{l,n}^{(i)}, \quad (24)$$

where the vectors $\vec{R}_{l,n}^{(i)}$ and $\vec{Q}_{l,n}^{(i)}$ represent all the R and Q messages in each non-zero block of the H matrix, $s(l,n)$ denotes the shift coefficient for the l^{th} block row and n^{th} non-zero block of the H matrix (note that null blocks in the H matrix need not be processed); $\left[\vec{R}_{l,n}^{i-1}\right]^{S(l,n)}$ denotes that the vector $\vec{R}_{l,n}^{i-1}$ is cyclically shifted up by the amount $s(l,n)$, and k is the check-node degree of the block row or the layer. A negative sign on $s(l,n)$ indicates that it is cyclic down shift (equivalent cyclic left shift). $f(\cdot)$ denotes the check-node processing.



163. The TDMP algorithm equations of the Accused Products are substantially identical to what is set forth in the '530 patent.

'530 Patent at 15:35–62

For the irregular block LDPC codes, the TDMP algorithm can be described with equations (21)-(24):

$\vec{R}_{l,n}^{(0)}=0, \vec{P}_n=\vec{L}_n^{(0)}$ [Initialization for each new received data frame],

$\forall i=1,2,\ldots,it_{max}$ [Iteration loop],

$\forall l=1,2,\ldots,j$ [Sub-iteration loop],

$\forall n=1,2,\ldots,k$ [Block column loop], (21)

$[\vec{Q}_{l,n}^{(i)}]^{S(l,n)}=[\vec{P}_n]^{S(l,n)}-\vec{R}_{l,n}^{(i-1)}$ (22)

$\vec{R}_{l,n'}^{(i)}=f([\vec{Q}_{l,n'}^{(i)}]^{S(l,n')}, \forall n'=1,2,\ldots,k).$ (23)

$[\vec{P}_n]^{S(l,n)}=[\vec{Q}_{l,n}^{(i)}]^{S(l,n)}+\vec{R}_{l,n}^{(i)},$ (24)

where the vectors and $\vec{R}_{l,n}^{(i)}$ and $\vec{Q}_{l,n}^{(i)}$ represent all the R and Q messages in each non-zero block of the H matrix, s(l,n) denotes the shift coefficient for the i^{th} block row and n^{th} non-zero block of the H matrix (note that null blocks in the H matrix need not be processed); $[\vec{R}_{l,n}^{i-1}]^{S(l,n)}$ denotes that the vector is cyclically shifted up by the amount s(l,n) and k is the check-node degree of the block row or the layer. A negative sign on s(l,n) indicates that it is cyclic down shift (equivalent cyclic left shift). $f(\cdot)$ denotes the check-node processing, which can be performed using BCJR, SP or MS.

Layered Decoder Presentation at 3

For the irregular block LDPC codes, the TDMP algorithm can be described with equations (21)-(24):

$\vec{R}_{l,n}^{(0)}=0, \vec{P}_n=\vec{L}_n^{(0)}$ [Initialization for each new received data frame], (21)

$\forall i=1,2,\cdots,it_{\max}$ [Iteration loop],

$\forall l=1,2,\cdots,j$ [Sub-iteration loop],

$\forall n=1,2,\cdots,k$ [Block column loop],

$[\vec{Q}_{l,n}^{(i)}]^{S(l,n)}=[\vec{P}_n]^{S(l,n)}-\vec{R}_{l,n}^{(i-1)},$ (22)

$\vec{R}_{l,n}^{(i)}=f([\vec{Q}_{l,n'}^{(i)}]^{S(l,n')}, \forall n'=1,2,\cdots,k),$ (23)

$[\vec{P}_n]^{S(l,n)}=[\vec{Q}_{l,n}^{(i)}]^{S(l,n)}+\vec{R}_{l,n}^{(i)},$ (24)

where the vectors $\vec{R}_{l,n}^{(i)}$ and $\vec{Q}_{l,n}^{(i)}$ represent all the R and Q messages in each non-zero block of the H matrix, $s(l,n)$ denotes the shift coefficient for the l^{th} block row and n^{th} non-zero block of the H matrix (note that null blocks in the H matrix need not be processed); $[\vec{R}_{l,n}^{i-1}]^{S(l,n)}$ denotes that the vector $\vec{R}_{l,n}^{i-1}$ is cyclically shifted up by the amount $s(l,n)$, and k is the check-node degree of the block row or the layer. A negative sign on $s(l,n)$ indicates that it is cyclic down shift (equivalent cyclic left shift). $f(\cdot)$ denotes the check-node processing.

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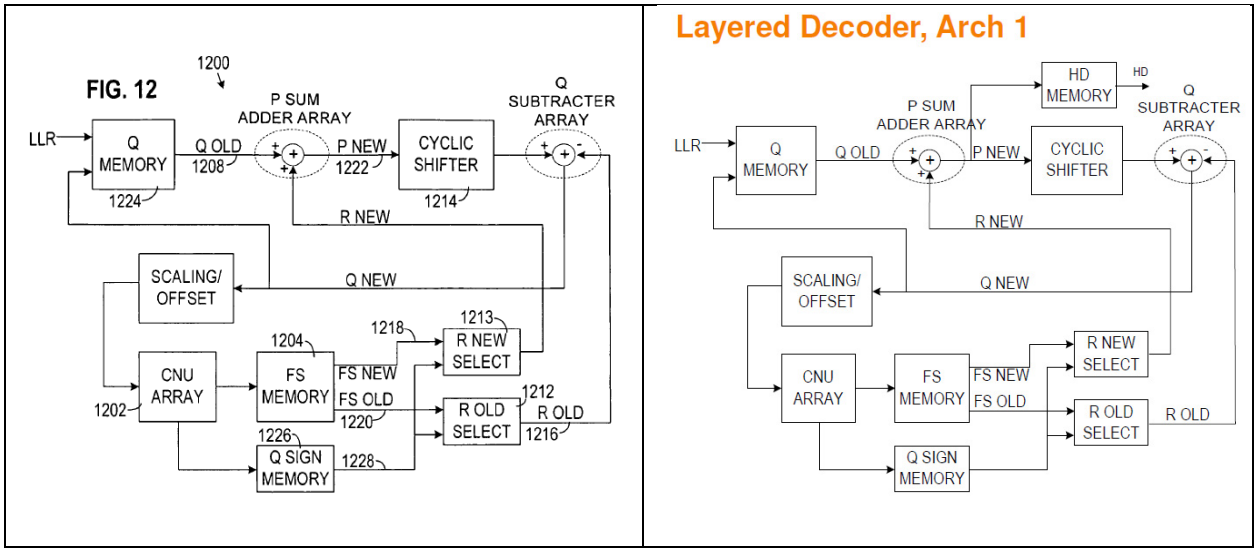
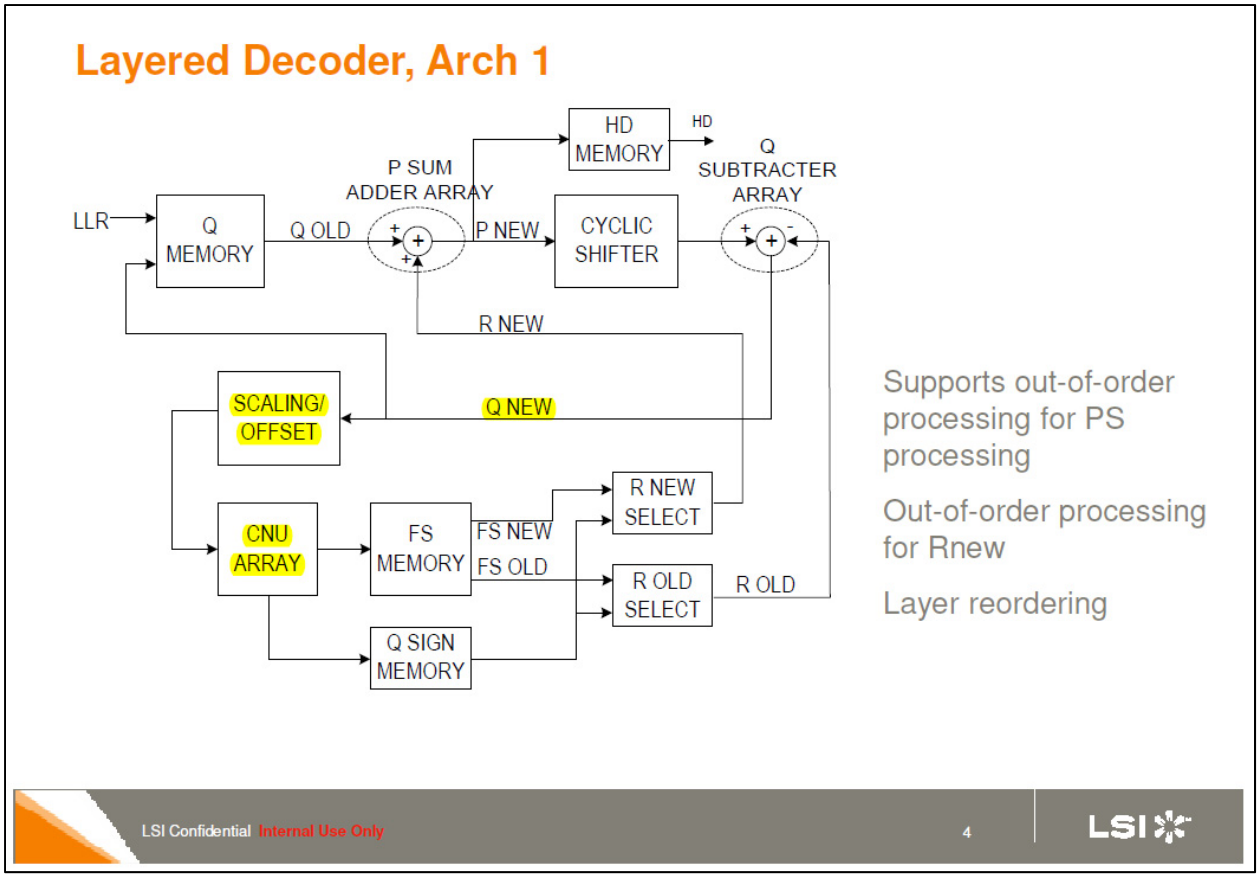
164. The layered decoder architecture of the Accused Products is substantially identical to what is set forth in the '530 patent.

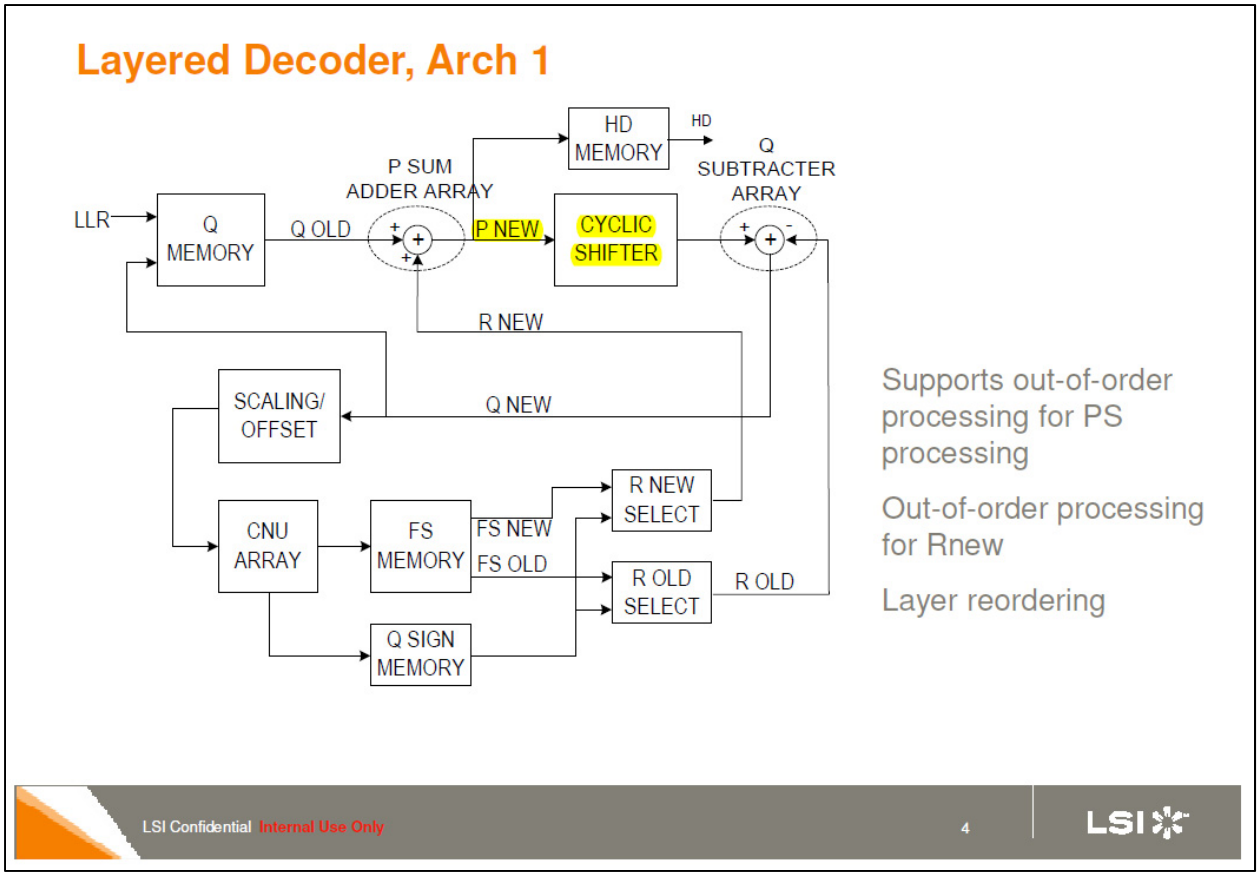
'530 Patent at FIG. 12 **Layered Decoder Presentation at 4**



165. The Accused Products include logic configured to reduce the magnitude a Q message provided to a check node unit of the decoder. For example, the Layered Decoder Presentation discloses the presence of a SCALING/OFFSET unit configured to reduce the magnitude of a Q message provided to a check node unit of the decoder.



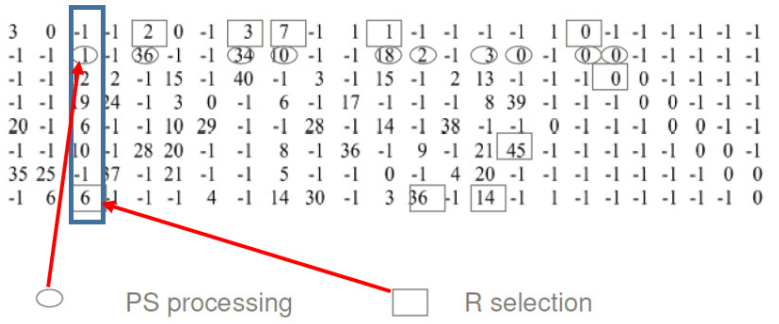
166. The Accused Products include a permuter configured to permute the P message by a difference of permutation of a block currently being processed and permutation of a block previously processed. For example, the Layered Decoder Presentation discloses the presence of CYCLIC SHIFTER configured to permute the P message by a difference of permutation of a block currently being processed and permutation of a block previously processed.



167. The Accused Products include wherein the block currently being processed and the block previously processed are in a same block column of an LDPC matrix. For example, the Layered Decoder Presentation discloses that the computation of the R messages ("R SELECTION") for a first non-zero block are generated while processing the second non-zero block ("PS PROCESSING"), and these two blocks are in a same block column of an LDPC matrix.

Out-of-order layer processing for R Selection

Rate 2/3 A code:



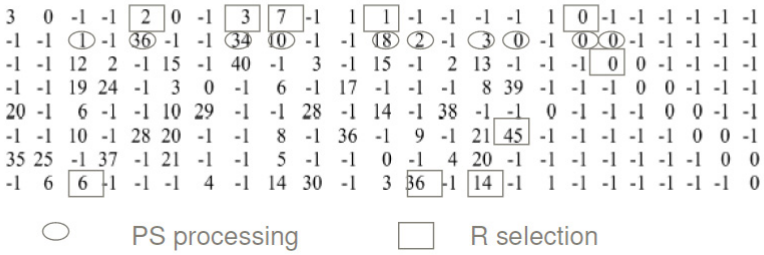
R selection is out-of-order so that it can feed the data required for the PS processing of the second layer.

So here we decoupled the execution of R new messages with the execution of CNU processing.

Here we execute the instruction/computation at precise moment when the result is needed!!!

Out-of-order block processing for Partial State

Rate 2/3 A code:



Re-ordering of block processing . While processing the layer 2,

the blocks which depend on layer 1 will be processed last to allow for the pipeline latency.

In the above example, the pipeline latency can be 5.

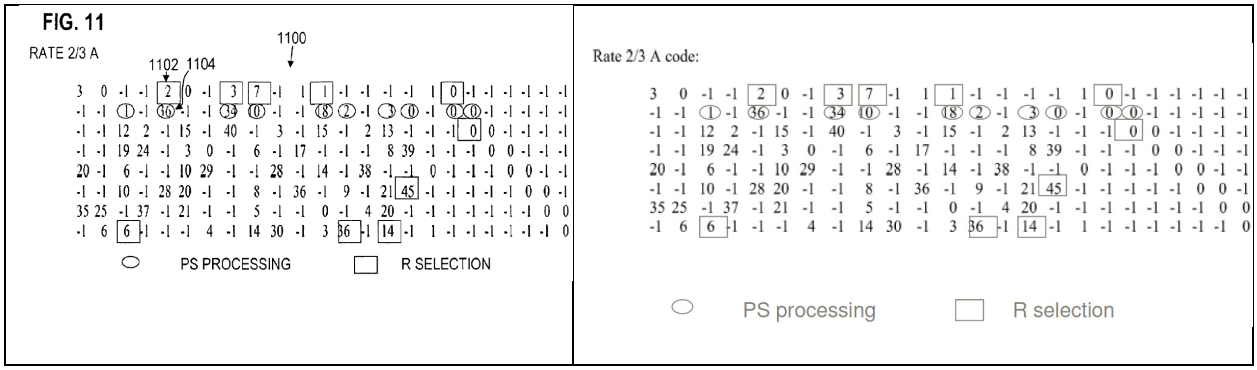
The vector pipeline depth is 5.so no stall cycles are needed while processing the layer 2 due to the pipelining. [In other implementations, the stall cycles are introduced – which will effectively reduce the throughput by a huge margin.]

Also we will sequence the operations in layer such that we process the block first that has dependent data available for the longest time.

This naturally leads us to true out-of-order processing across several layers. In practice we wont do out-of-order partial state processing involving more than 2 layers.

168. The exemplary Rate 2/3 A code of the Accused Products is identical to what is set forth in the '530 patent.

'530 Patent at FIG. 11 **Layered Decoder Presentation at 10**



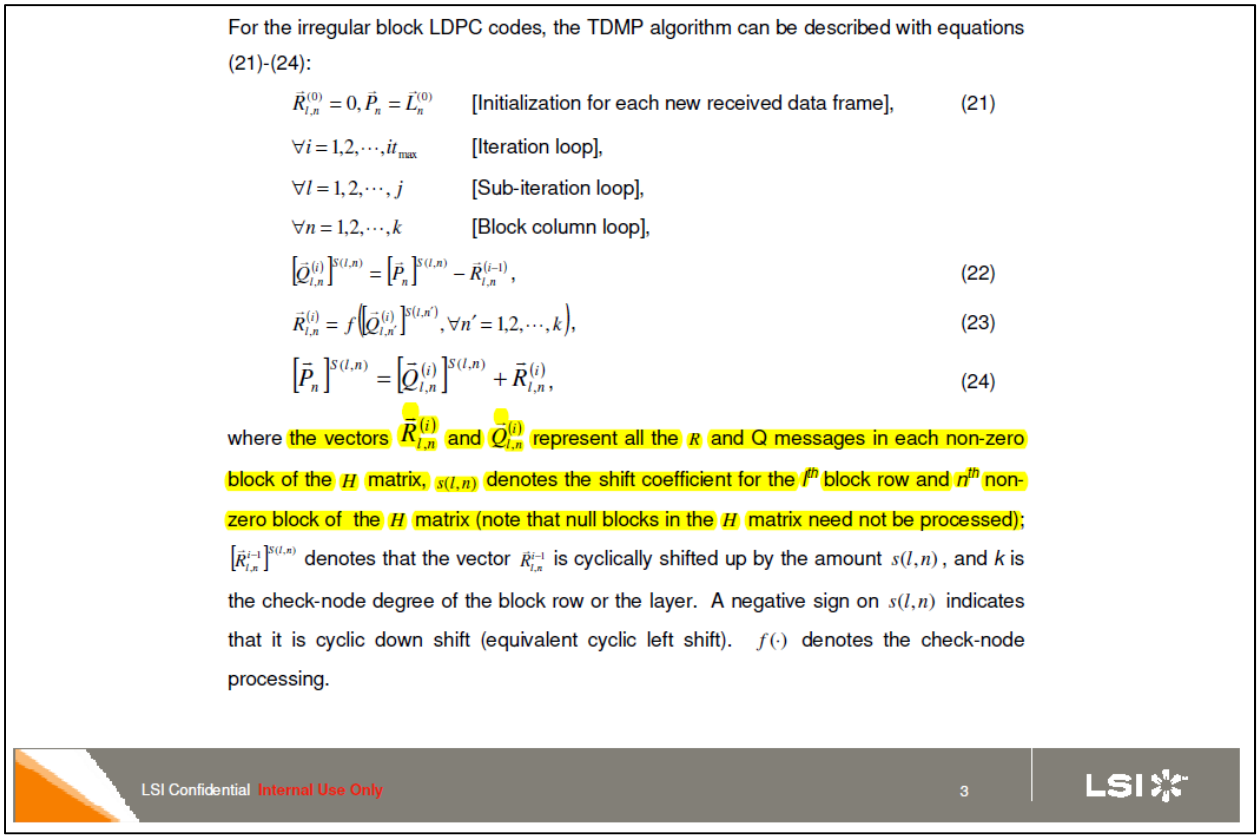
169. Claim 25 of the '530 patent recites as follows:

> 25. A low density parity check (LDPC) code decoder, comprising:
> a control unit that controls decoder processing, the control unit configured to cause the decoder to process blocks of an LDPC matrix in a sequence defined by an order of non-zero blocks of a given layer of the LDPC matrix;
> wherein the LDPC matrix comprises a plurality of layers, each layer having a plurality of blocks ordered such that the sequence of non-zero blocks of the given layer of the LDPC matrix specifies a first set of non-zero blocks of the given layer to be processed at a given time and a second set of non-zero blocks of the given layer to be processed after the first set of non-zero blocks; wherein the first set specifies only non-zero blocks of the given layer that are not dependent on a result of a previously processed layer and the second set specifies non-zero blocks of the given layer that are dependent on a result of the previously processed layer.

170. On information and belief, the Accused Products satisfy each and every limitation of Claim 25. The Accused Products include an LDPC code decoder. *See* ¶ 166, 91, *supra*.

171. The Accused Products include a control unit that controls decoder processing and that is configured to cause the decoder to process blocks of an LDPC matrix in a sequence defined by an order of non-zero blocks of a given layer of the LDPC matrix. For example, using

disclosures taken directly from the '530 patent, the Layered Decoder Presentation indicates that the Accused Products process blocks of an LDPC matrix in a sequence defined by an order of non-zero blocks of a given layer of the LDPC matrix.



For the irregular block LDPC codes, the TDMP algorithm can be described with equations (21)-(24):

$\vec{R}_{l,n}^{(0)} = 0, \vec{P}_n = \vec{L}_n^{(0)}$ [Initialization for each new received data frame], (21)

$\forall i = 1,2,\cdots,it_{\max}$ [Iteration loop],

$\forall l = 1,2,\cdots,j$ [Sub-iteration loop],

$\forall n = 1,2,\cdots,k$ [Block column loop],

$$\left[\vec{Q}_{l,n}^{(i)}\right]^{S(l,n)} = \left[\vec{P}_n\right]^{S(l,n)} - \vec{R}_{l,n}^{(i-1)}, \quad (22)$$

$$\vec{R}_{l,n}^{(i)} = f\left(\left[\vec{Q}_{l,n'}^{(i)}\right]^{S(l,n')}, \forall n' = 1,2,\cdots,k\right), \quad (23)$$

$$\left[\vec{P}_n\right]^{S(l,n)} = \left[\vec{Q}_{l,n}^{(i)}\right]^{S(l,n)} + \vec{R}_{l,n}^{(i)}, \quad (24)$$

where the vectors $\vec{R}_{l,n}^{(i)}$ and $\vec{Q}_{l,n}^{(i)}$ represent all the R and Q messages in each non-zero block of the H matrix, $s(l,n)$ denotes the shift coefficient for the l^{th} block row and n^{th} non-zero block of the H matrix (note that null blocks in the H matrix need not be processed); $\left[\vec{R}_{l,n}^{i-1}\right]^{S(l,n)}$ denotes that the vector $\vec{R}_{l,n}^{i-1}$ is cyclically shifted up by the amount $s(l,n)$, and k is the check-node degree of the block row or the layer. A negative sign on $s(l,n)$ indicates that it is cyclic down shift (equivalent cyclic left shift). $f(\cdot)$ denotes the check-node processing.

172. The TDMP algorithm equations of the Accused Products are identical to what is set forth in the '530 patent.

'530 Patent at 15:35–62

For the irregular block LDPC codes, the TDMP algorithm can be described with equations (21)-(24):

$\vec{R}_{l,n}^{(0)}=0, \vec{P}_n=\vec{L}_n^{(0)}$ [Initialization for each new received data frame],

$\forall i=1,2,\ldots,it_{max}$ [Iteration loop],

$\forall l=1,2,\ldots,j$ [Sub-iteration loop],

$\forall n=1,2,\ldots,k$ [Block column loop], (21)

$[\vec{Q}_{l,n}^{(i)}]^{S(l,n)}=[\vec{P}_n]^{S(l,n)}-\vec{R}_{l,n}^{(i-1)}$ (22)

$\vec{R}_{l,n}^{(i)}=f([\vec{Q}_{l,n'}^{(i)}]^{S(l,n')}, \forall n'=1,2,\ldots,k).$ (23)

$[\vec{P}_n]^{S(l,n)}=[\vec{Q}_{l,n}^{(i)}]^{S(l,n)}+\vec{R}_{l,n}^{(i)},$ (24)

where the vectors and $\vec{R}_{l,n}^{(i)}$ and $\vec{Q}_{l,n}^{(i)}$ represent all the R and Q messages in each non-zero block of the H matrix, s(l,n) denotes the shift coefficient for the i^{th} block row and n^{th} non-zero block of the H matrix (note that null blocks in the H matrix need not be processed); $[\vec{R}_{l,n}^{i-1}]^{S(l,n)}$ denotes that the vector is cyclically shifted up by the amount s(l,n) and k is the check-node degree of the block row or the layer. A negative sign on s(l,n) indicates that it is cyclic down shift (equivalent cyclic left shift). $f(\cdot)$ denotes the check-node processing, which can be performed using BCJR, SP or MS.

Layered Decoder Presentation at 3

For the irregular block LDPC codes, the TDMP algorithm can be described with equations (21)-(24):

$\vec{R}_{l,n}^{(0)}=0, \vec{P}_n=\vec{L}_n^{(0)}$ [Initialization for each new received data frame], (21)

$\forall i=1,2,\cdots,it_{\max}$ [Iteration loop],

$\forall l=1,2,\cdots,j$ [Sub-iteration loop],

$\forall n=1,2,\cdots,k$ [Block column loop],

$[\vec{Q}_{l,n}^{(i)}]^{S(l,n)}=[\vec{P}_n]^{S(l,n)}-\vec{R}_{l,n}^{(i-1)},$ (22)

$\vec{R}_{l,n}^{(i)}=f\left([\vec{Q}_{l,n'}^{(i)}]^{S(l,n')}, \forall n'=1,2,\cdots,k\right),$ (23)

$[\vec{P}_n]^{S(l,n)}=[\vec{Q}_{l,n}^{(i)}]^{S(l,n)}+\vec{R}_{l,n}^{(i)},$ (24)

where the vectors $\vec{R}_{l,n}^{(i)}$ and $\vec{Q}_{l,n}^{(i)}$ represent all the R and Q messages in each non-zero block of the H matrix, $s(l,n)$ denotes the shift coefficient for the l^{th} block row and n^{th} non-zero block of the H matrix (note that null blocks in the H matrix need not be processed); $[\vec{R}_{l,n}^{i-1}]^{S(l,n)}$ denotes that the vector $\vec{R}_{l,n}^{i-1}$ is cyclically shifted up by the amount $s(l,n)$, and k is the check-node degree of the block row or the layer. A negative sign on $s(l,n)$ indicates that it is cyclic down shift (equivalent cyclic left shift). $f(\cdot)$ denotes the check-node processing.

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173. The Accused Products include wherein the LDPC matrix comprises a plurality of layers, each layer having a plurality of blocks ordered such that the sequence of non-zero blocks of the given layer of the LDPC matrix specifies a first set of non-zero blocks of the given layer to be processed at a given time and a second set of non-zero blocks of the given layer to be processed after the first set of non-zero blocks. For example, upon information and belief, the Spyder product includes a layered decoder wherein each layer of the LDPC matrix is constructed such that non-zero blocks that are not dependent on the previous layer occur at earlier locations in the layer than non-zero blocks that are dependent on the previous layer. Further, upon information and belief, non-zero blocks of a given layer of the LDPC matrix in the layered decoder of the Spyder product are processed in the order in which they occur in the layer.

174. The Accused Products include wherein the first set specifies only non-zero blocks of the given layer that are not dependent on a result of a previously processed layer and the second set specifies non-zero blocks of the given layer that are dependent on a result of the previously processed layer. For example, upon information and belief, the Spyder product includes a layered decoder wherein each layer of the LDPC matrix is constructed such that non-zero blocks that are not dependent on the previous layer occur at earlier locations in the layer than non-zero blocks that are dependent on the previous layer.

175. In view of the foregoing, the Accused Products directly infringe at least Claims 13-20, 22-23, and 25-31 of the '530 patent.

176. On information and belief, Defendant and/or the Broadcom Predecessor Entities have had actual or constructive knowledge of the '530 patent since at least August 18, 2015.

177. Defendant further has knowledge of the '530 patent at least as early as the filing and/or service of this Complaint. Defendant has further been aware that use of the Accused Products necessarily practice the inventions in Claims 13-20, 22-23, and 25-31 of the '530 patent.

178. On information and belief, Defendant and/or the Broadcom Predecessor Entities have taken active steps to induce infringement by others of at least Claims 13-20, 22-23, and 25-31 of the '530 patent in violation of 35 U.S.C. §271(b), including, for example, by (a) inducing manufacturers to practice the claims, and (b) inducing end users to practice the claims. Such active steps include, but are not limited to, selling Accused Products with the knowledge and intent that the Accused Products will be used, imported, or operated in violation of the '530 patent.

179. On information and belief, Defendant and/or the Broadcom Predecessor Entities have known or should have known that such activities induce others to directly infringe one or more of at least Claims 13-20, 22-23, and 25-31 of the '530 patent. For example, Defendant and/or the Broadcom Predecessor Entities should have known that their actions induced others to directly infringe as of the date it became aware of the issuance of the '530 patent on or about August 18, 2015, and in any event no later than the date of service of this complaint. Defendant and/or the Broadcom Predecessor Entities were further informed that the technology in the Accused Products infringed the '530 patent, and Defendant and/or the Broadcom Predecessor Entities have knowingly and purposefully continued to exploit the patented technology despite knowing that it was covered by the '530 patent. Defendant is further aware that the Accused Products necessarily practice Claims 13-20, 22-23, and 25-31 of the '530 patent.

180. On information and belief, Defendant and/or the Broadcom Predecessor Entities have contributed to the infringement of at least Claims 13-20, 22-23, and 25-31 of the '530 patent by others, including consumer/end-user sale, importation, or use of the Accused Products, in violation of 35 U.S.C. § 271(c). Acts by Defendant and/or the Broadcom Predecessor Entities that contribute to the infringement by others include, but are not limited to, the sale, offer for sale, and/or import by Defendant of the Accused Products. Such Accused Products are especially made for or adapted for use to infringe, and are not a staple article of commerce and are not suitable for substantial non-infringing use. As also described above, Defendant has, on information and belief, been on notice of the '140 patent since at least the filing of this complaint and likely at or near its issuance in view of the knowledge set forth above regarding the '530 patents related patents. Defendant is further aware that the Accused Products necessarily practice Claims 13-20, 22-23, and 25-31 of the '530 patent.

181. The Accused Products are especially made for or adapted for use to infringe, and are not a staple article of commerce and are not suitable for substantial non-infringing use. By way of example, the use of the LDPC decoders included in the Accused Products is necessary to use the accused products for their intended purpose (decoding data from a hard disk drive, solid state drive, or wireless digital transmission), and the LDPC decoders necessarily perform the claimed inventions when they decode data. Accordingly, the Accused Products do not have a substantial use that does not entail practicing the claimed inventions. On information and belief, the Accused Products cannot be used but to infringe the '530 patent.

182. Despite Defendant's knowledge, notice, and ongoing infringement of the '530 patent, Defendant continues to sell, offer for sale, important, test, or use the Accused Products in a manner that willfully infringes the '530 patent, and on information and belief continues to sell and/or offer for sale the Accused Products to the United States market for customers / end users to infringe. Defendant's infringement of the '530 patent is willful, as set forth above. Defendant lacks a justifiable belief that it does not infringe the '530 patent, or that the '530 patent is invalid or unenforceable, and has acted recklessly in its infringing activity, justifying an increase in the damages to be awarded to Plaintiff up to three times the amount found or assessed, in accordance with 35 U.S.C. § 284.

183. This case is rendered an exceptional case at least in light of Defendant's willful infringement of the '530 patent, justifying an award to Plaintiff of its reasonable attorney fees, in accordance with 35 U.S.C. § 285.

184. Defendant has no adequate remedy at law for Defendant's acts of infringement. As a direct and proximate result of Defendant's acts of infringement, Plaintiff has suffered and

continues to suffer damages and irreparable harm. Unless Defendant's acts of infringement are enjoined by this Court, Plaintiff will continue to be damaged and irreparably harmed.

185. Defendant's infringement of the '530 patent has damaged and continues to damage Plaintiff in an amount yet to be determined, of at least a reasonable royalty and/or lost profits that Plaintiff would have made but for Defendant's infringement acts.

COUNT IV
(Infringement under 35 U.S.C. § 271 of U.S. Patent No. 8,359,522)

186. Plaintiff repeats and re-alleges the paragraphs above as if fully set forth herein.

187. The '522 patent is valid, enforceable, and was duly issued on January 22, 2013 in full compliance with Title 35 of the United States Code.

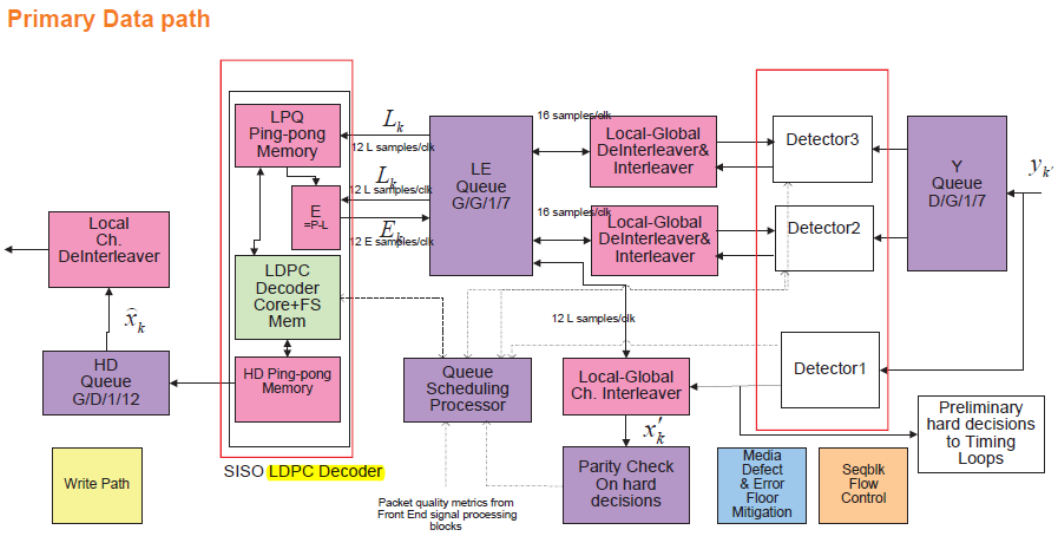
188. On information and belief, in violation of 35 U.S.C. § 271, Defendant and/or the Broadcom Predecessor Entities have infringed, contributed to the infringement of, and/or induced others to infringe the '522 patent, either literally or under the doctrine of equivalents, by, among other things, making, using, offering for sale, selling, and/or importing into the United States unlicensed systems and/or products in a manner that infringes at least Claims 85-97 of the '522 patent.

189. On information and belief, Defendant and/or the Broadcom Predecessor Entities have directly infringed the '522 patent, for example, by making, using, selling, offering to sell, and/or importing into the United States the Accused Products, which meet each and every limitation of at least Claim 85 of the '522 patent, in violation of Plaintiff's patent rights and without Plaintiff's license or authority. Non-limiting examples of such infringement are provided below, based on the limited information currently available to Plaintiff.

190. Claim 85 of the '522 patent recites as follows:

> 85. A method for decoding a low density parity check code, comprising:
> selecting a first R message from a plurality of previously generated possible R messages based on at least a message index value and a sign bit;
> generating a Q message by combining the first R message with a P message;
> cyclically shifting the P message; and
> updating the P message responsive to determination of a final state for each block row.

191. On information and belief, the Accused Products satisfy each and every limitation of Claim 85. The Accused Products decode a low density parity check code. For example, the McLaren Architecture Presentation references the LDPC decoder.



The primary data-path contains one SISO LDPC decoder and three detectors.
The LDPC decoder is designed such that it can handle the total amount of 15 local layered iterations in three global iterations for each codeword.
Each Detector operate on a different packet ensuring one code word(or packet) can be processed in the inter-arrival time T. Each detector processes 4 samples per clock cycle.
Thus both the detector and the LDPC decoder can sustain maximum of three global iterations per each codeword if no statistical buffering is employed.

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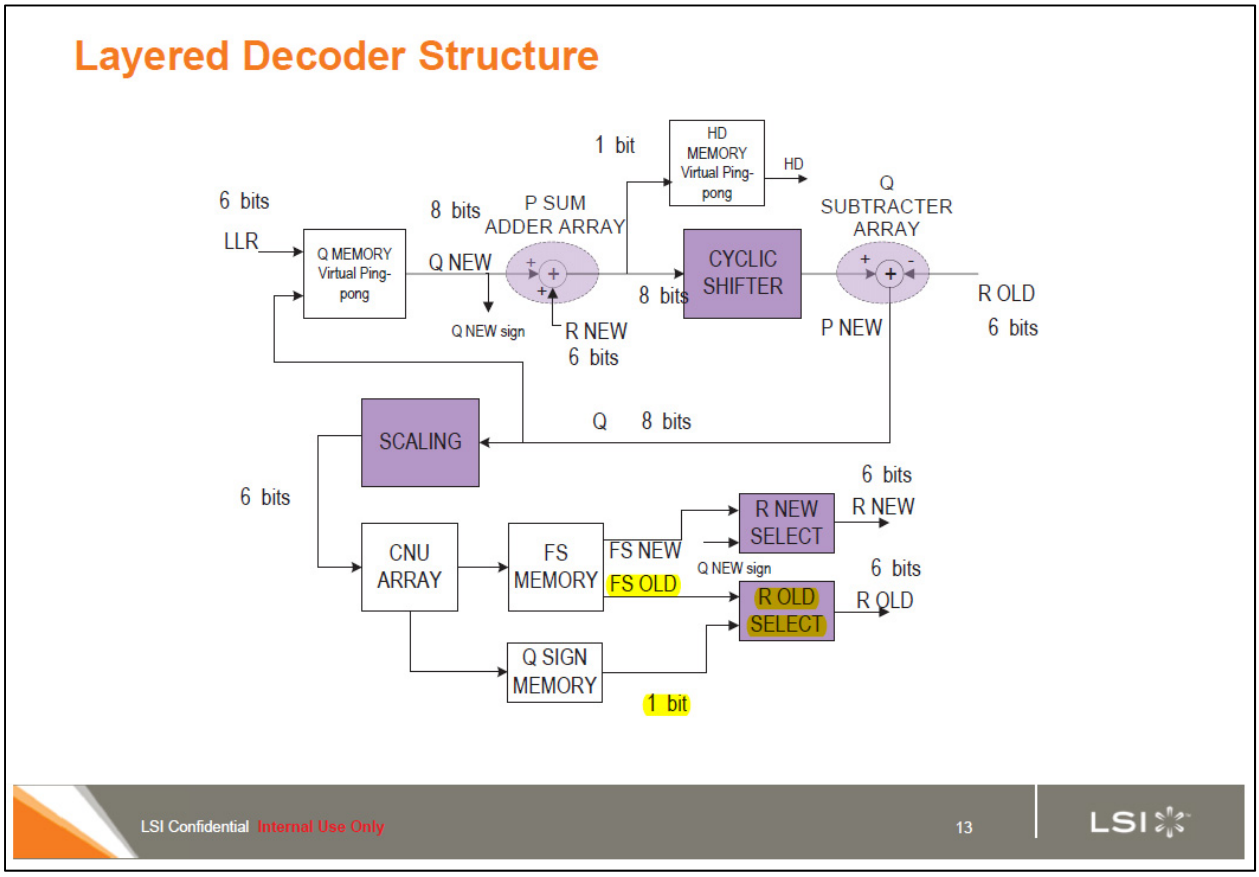
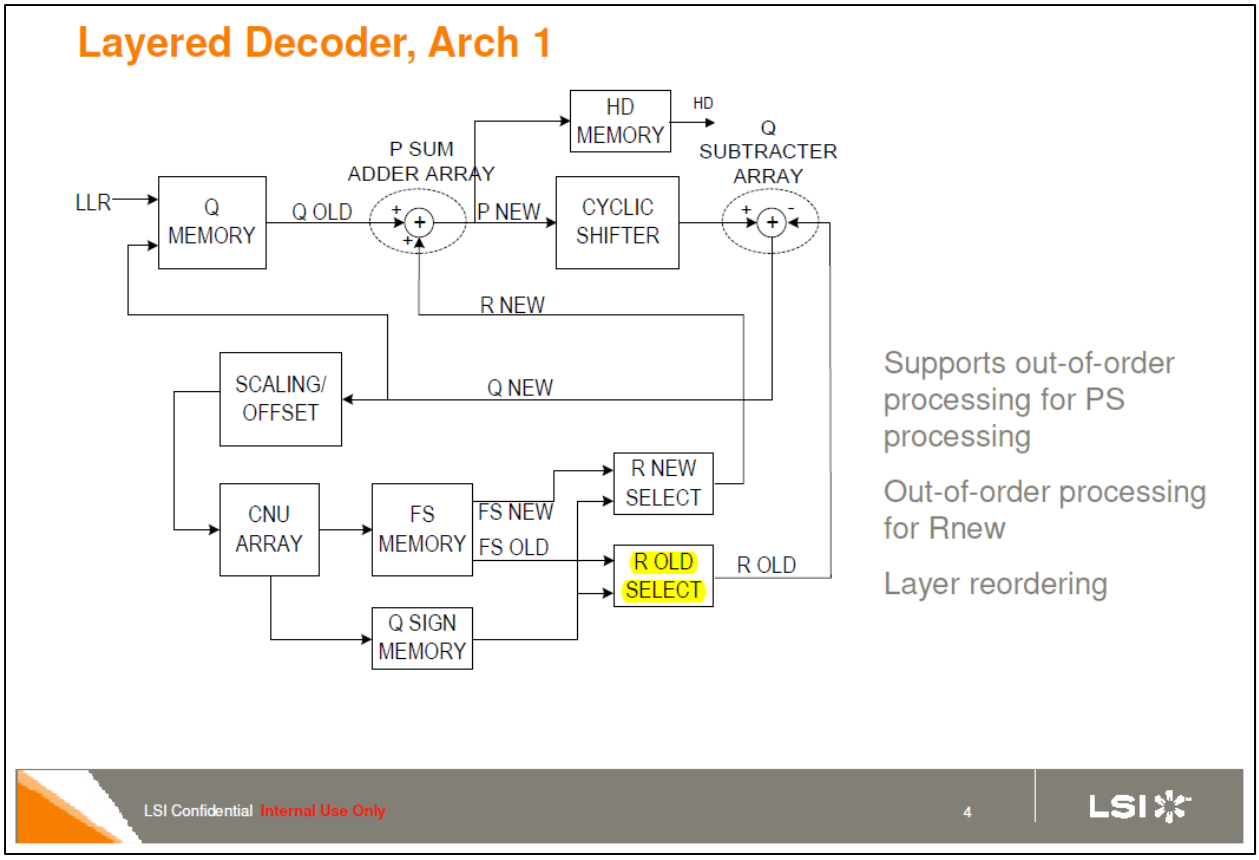
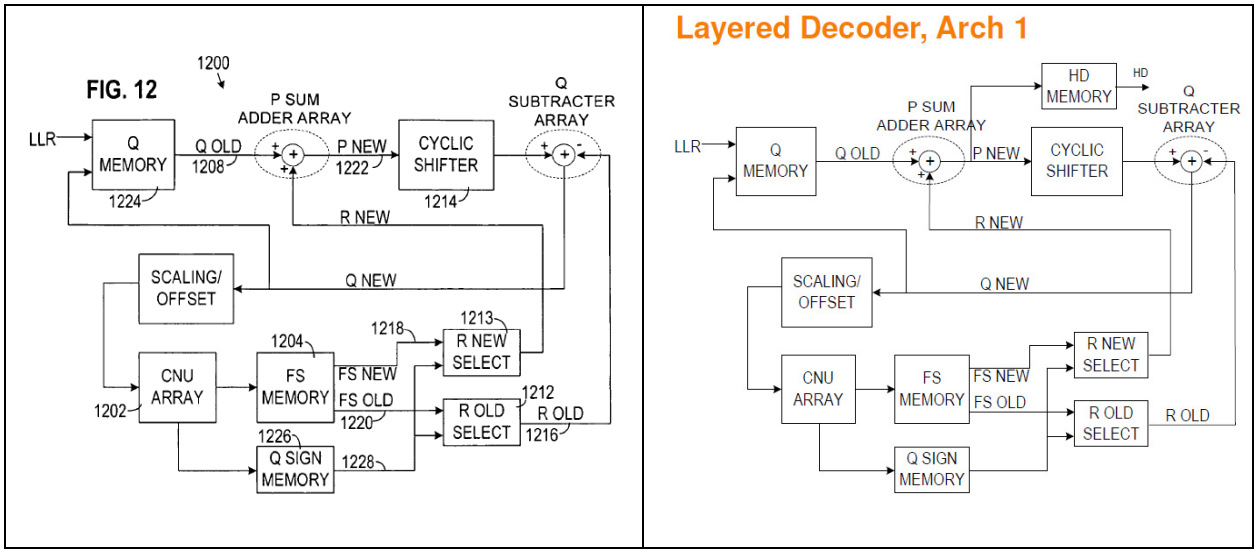
192. The Accused Products select a first R message from a plurality of previously generated possible R messages based on at least a message index value and a sign bit. For example, the McLaren Architecture Presentation and the Layered Decoder Presentation each disclose the presence of an R OLD SELECT unit that selects a first R message from a plurality of previously generated possible R messages based on at least a message index value and a sign bit.





193. The layered decoder architecture of the Accused Products is identical to what is set forth in the '522 patent.

'522 Patent at FIG. 12 **Layered Decoder Presentation at 4**



194. The Accused Products generate a Q message by combining the first R message with a P message. For example, the Layered Decoder Presentation discloses a Q SUBTRACTER ARRAY that generates a Q message by combining the first R message with a P message.

For the irregular block LDPC codes, the TDMP algorithm can be described with equations (21)-(24):

$\vec{R}_{l,n}^{(0)} = 0, \vec{P}_n = \vec{L}_n^{(0)}$ [Initialization for each new received data frame], (21)

$\forall i = 1,2,\cdots,it_{\max}$ [Iteration loop],

$\forall l = 1,2,\cdots,j$ [Sub-iteration loop],

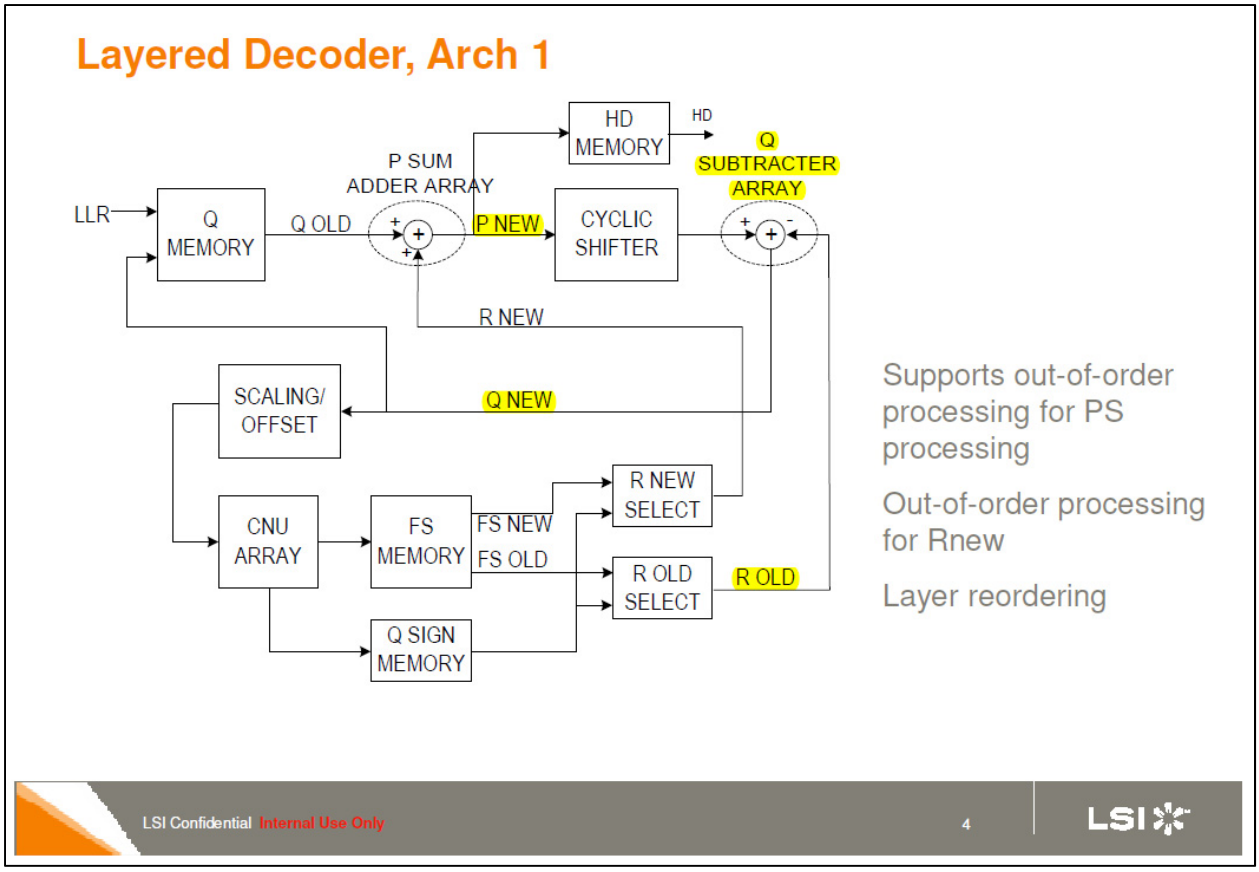
$\forall n = 1,2,\cdots,k$ [Block column loop],

$$\left[\vec{Q}_{l,n}^{(i)}\right]^{S(l,n)} = \left[\vec{P}_n\right]^{S(l,n)} - \vec{R}_{l,n}^{(i-1)}, \quad (22)$$

$$\vec{R}_{l,n}^{(i)} = f\left(\left[\vec{Q}_{l,n'}^{(i)}\right]^{S(l,n')}, \forall n' = 1,2,\cdots,k\right), \quad (23)$$

$$\left[\vec{P}_n\right]^{S(l,n)} = \left[\vec{Q}_{l,n}^{(i)}\right]^{S(l,n)} + \vec{R}_{l,n}^{(i)}, \quad (24)$$

where the vectors $\vec{R}_{l,n}^{(i)}$ and $\vec{Q}_{l,n}^{(i)}$ represent all the R and Q messages in each non-zero block of the H matrix, $s(l,n)$ denotes the shift coefficient for the l^{th} block row and n^{th} non-zero block of the H matrix (note that null blocks in the H matrix need not be processed); $\left[\vec{R}_{l,n}^{i-1}\right]^{S(l,n)}$ denotes that the vector $\vec{R}_{l,n}^{i-1}$ is cyclically shifted up by the amount $s(l,n)$, and k is the check-node degree of the block row or the layer. A negative sign on $s(l,n)$ indicates that it is cyclic down shift (equivalent cyclic left shift). $f(\cdot)$ denotes the check-node processing.



195. The TDMP algorithm equations of the Accused Products are identical to what is set forth in the '522 patent.

'522 Patent at 15:23–50

For the irregular block LDPC codes, the TDMP algorithm can be described with equations (21)-(24):

$\vec{R}_{l,n}^{(0)}=0, \vec{P}_n=\vec{L}_n^{(0)}$ [Initialization for each new received data frame],

$\forall i=1,2,\ldots,it_{max}$ [Iteration loop],

$\forall l=1,2,\ldots,j$ [Sub-iteration loop],

$\forall n=1,2,\ldots,k$ [Block column loop], (21)

$[\vec{Q}_{l,n}^{(i)}]^{S(l,n)}=[\vec{P}_n]^{S(l,n)}-\vec{R}_{l,n}^{i-1)}$, (22)

$\vec{R}_{l,n}^{(i)}=f([\vec{Q}_{l,n}^{(i)}]^{S(l,n')}), \forall n'=1,2,\ldots,k)$, (23)

$[\vec{P}_n]^{S(l,n)}=[\vec{Q}_{l,n}^{(i)}]^{S(l,n)}+\vec{R}_{l,n}^{(i)}$, (24)

where the vectors $\vec{R}_{l,n}^{(i)}$ and $\vec{Q}_{l,n}^{(i)}$ represent all the R and Q messages in each non-zero block of the H matrix, s(l,n) denotes the shift coefficient for the l^{th} block row and n^{th} non-zero block of the H matrix (note that null blocks in the H matrix need not be processed); $[\vec{R}_{l,n}^{i-1}]^{S(l,n)}$ denotes that the vector $\vec{R}_{l,n}^{i-1}$ is cyclically shifted up by the amount s(l,n), and k is the check-node degree of the block row or the layer. A negative sign on s(l,n) indicates that it is cyclic down shift (equivalent cyclic left shift). f(•) denotes the check-node processing, which can be performed using BCJR, SP or MS.

Layered Decoder Presentation at 3

For the irregular block LDPC codes, the TDMP algorithm can be described with equations (21)-(24):

$\vec{R}_{l,n}^{(0)}=0, \vec{P}_n=\vec{L}_n^{(0)}$ [Initialization for each new received data frame], (21)

$\forall i=1,2,\cdots,it_{\max}$ [Iteration loop],

$\forall l=1,2,\cdots,j$ [Sub-iteration loop],

$\forall n=1,2,\cdots,k$ [Block column loop],

$\left[\vec{Q}_{l,n}^{(i)}\right]^{S(l,n)}=\left[\vec{P}_n\right]^{S(l,n)}-\vec{R}_{l,n}^{(i-1)}$, (22)

$\vec{R}_{l,n}^{(i)}=f\left(\left[\vec{Q}_{l,n}^{(i)}\right]^{S(l,n')}, \forall n'=1,2,\cdots,k\right)$, (23)

$\left[\vec{P}_n\right]^{S(l,n)}=\left[\vec{Q}_{l,n}^{(i)}\right]^{S(l,n)}+\vec{R}_{l,n}^{(i)}$, (24)

where the vectors $\vec{R}_{l,n}^{(i)}$ and $\vec{Q}_{l,n}^{(i)}$ represent all the R and Q messages in each non-zero block of the H matrix, $s(l,n)$ denotes the shift coefficient for the l^{th} block row and n^{th} non-zero block of the H matrix (note that null blocks in the H matrix need not be processed); $\left[\vec{R}_{l,n}^{i-1}\right]^{S(l,n)}$ denotes that the vector $\vec{R}_{l,n}^{i-1}$ is cyclically shifted up by the amount $s(l,n)$, and k is the check-node degree of the block row or the layer. A negative sign on $s(l,n)$ indicates that it is cyclic down shift (equivalent cyclic left shift). $f(\cdot)$ denotes the check-node processing.

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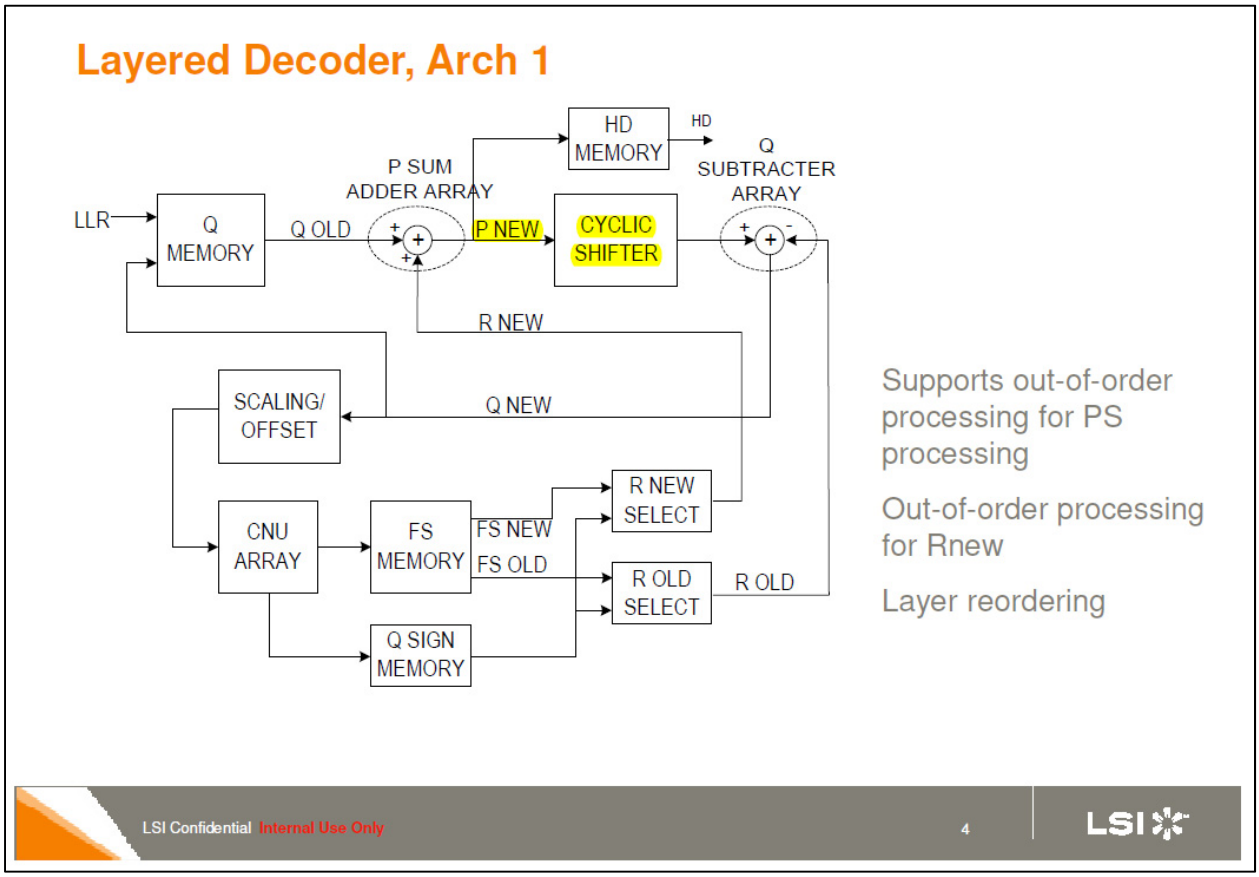
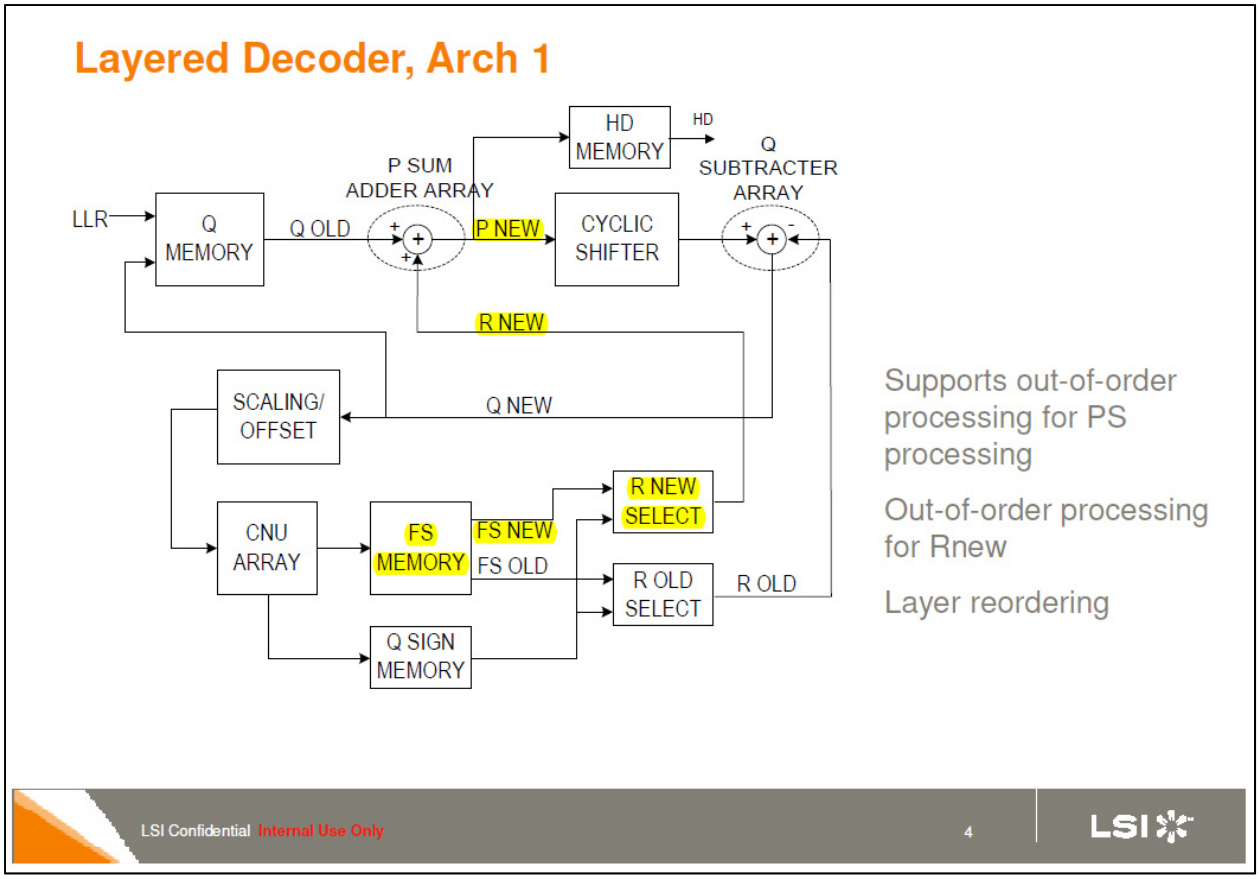
196. The Accused Products cyclically shift the P message. For example, the Layered Decoder Presentation discloses a CYCLIC SHIFTER that shifts the P Message.



197. The Accused Products update the P message responsive to determination of a final state for each block row. For example, the Layered Decoder Presentation discloses that for each block row, each P message is a function of R NEW, and R NEW is based on a determination of a final state for the row.



198. In view of the foregoing, the Accused Products directly infringe at least Claims 85-97 of the '522 patent through Defendant's and/or Broadcom Predecessor Entities' internal use and testing of the Accused Products.

199. On information and belief, Defendant and/or Broadcom Predecessor Entities had actual or constructive knowledge of the '522 patent since at least January 22, 2013.

200. Defendant further has knowledge of the '522 patent at least as early as the filing and/or service of this Complaint. Defendant is further aware that the Accused Products necessarily practice Claims 85-97 of the '522 patent.

201. On information and belief, Defendant and/or Broadcom Predecessor Entities have taken active steps to induce infringement by others of at least Claims 85-97 of the '522 patent in violation of 35 U.S.C. §271(b), including, for example, by (a) inducing manufacturers to perform

the claimed inventions when testing the Accused Products, and (b) inducing end users to perform the claimed inventions when using the Accused Products. Such active steps include, but are not limited to, selling Accused Products with the knowledge and intent that the Accused Products will be operated by such manufacturers and their customers in accordance with the claimed inventions.

202. On information and belief, Defendant and/or Broadcom Predecessor Entities knew or should have known that such activities induce others to directly infringe one or more of at least Claims 85-97 of the '522 patent. For example, Defendant and/or Broadcom Predecessor Entities should have known that their actions induced others to directly infringe as of the date LSI became aware of the issuance of the '522 patent on or about January 22, 2013, the date LSI was advised of the issuance of the '522 patent by Dr. Gunnam. Defendant and/or Broadcom Predecessor Entities were further informed that the technology in the Accused Products infringed the '522 patent, and Defendant and/or Broadcom Predecessor Entities knowingly and purposefully continued to exploit the patented technology despite knowing that it was covered by the '522 patent.

203. On information and belief, Defendant and/or Broadcom Predecessor Entities have contributed to the infringement of at least Claims 85-97 of the '522 patent by others, including consumer/end-user use of the Accused Products, in violation of 35 U.S.C. § 271(c). Acts by Defendant and/or Broadcom Predecessor Entities that contribute to the infringement of others include, but are not limited to, the sale, offer for sale, and/or import by Defendant of the Accused Products. Such Accused Products are especially made for or adapted for use to infringe, and are not a staple article of commerce and are not suitable for substantial non-infringing use. The Accused Products are apparatuses for use in practicing the inventions patented in Claims 85-97

of the '522 patent, and are at least a material part of those claimed inventions, for example, as described above with respect to claim 85. On information and belief, the steps recited in Claim 85, for example, are performed by the Accused Products.

204. As also described above, Defendant and/or Broadcom Predecessor Entities have, on information and belief, been on notice of the '522 patent since January 22, 2013 and in addition since filing and/or service of this Complaint. Defendant and/or Broadcom Predecessor Entities have further been aware that use of the Accused Products necessarily practice the inventions in Claims 85-97 of the '522 patent.

205. The Accused Products are especially made for or adapted for use to infringe, and are not a staple article of commerce and are not suitable for substantial non-infringing use. By way of example, the use of the LDPC decoders included in the Accused Products is necessary to use the accused products for their intended purpose (decoding data from a hard disk drive, solid state drive, or wireless digital transmission), and the LDPC decoders necessarily perform the claimed inventions when they decode data. Accordingly, the Accused Products do not have a substantial use that does not entail practicing the claimed inventions. On information and belief, the Accused Products cannot be used but to infringe the '522 patent.

206. Despite Defendant's knowledge, notice, and ongoing infringement of the '522 patent, Defendant continues to test or use the Accused Products in a manner that willfully infringes the '522 patent, and on information and belief continues to sell and/or offer for sale the Accused Products to the United States market for customers / end users to infringe. Defendant's infringement of the '522 patent is willful, as set forth above. Defendant lacks a justifiable belief that it does not infringe the '522 patent, or that the '140 patent is invalid or unenforceable, and

has acted recklessly in its infringing activity, justifying an increase in the damages to be awarded to Plaintiff up to three times the amount found or assessed, in accordance with 35 U.S.C. § 284.

207. This case is rendered an exceptional case at least in light of Defendant's willful infringement of the '140 patent, justifying an award to Plaintiff of its reasonable attorney fees, in accordance with 35 U.S.C. § 285.

208. Plaintiff has no adequate remedy at law for Defendant's acts of infringement. As a direct and proximate result of Defendant's acts of infringement, Plaintiff has suffered and continues to suffer damages and irreparable harm. Unless Defendant's acts of infringement are enjoined by this Court, Plaintiff will continue to be damaged and irreparably harmed.

209. Defendant's and/or Broadcom Predecessor Entities' infringement of the '522 patent has damaged and continues to damage Plaintiff in an amount yet to be determined, of at least a reasonable royalty and/or lost profits that Plaintiff would have made but for Defendant's and/or Broadcom Predecessor Entities' infringing acts.

COUNT V
(Infringement under 35 U.S.C. § 271 of U.S. Patent No. 8,656,250)

210. Plaintiff repeats and re-alleges the paragraph above as if fully set forth herein.

211. The '250 patent is valid, enforceable, and was duly issued on February 18, 2014 in full compliance with Title 35 of the United States Code.

212. On information and belief, in violation of 35 U.S.C. § 271, Defendant has infringed, contributed to the infringement of, and/or induced others to infringe the '250 patent, either literally or under the doctrine of equivalents, by, among other things, making, using, offering for sale, selling, and/or importing into the United States unlicensed systems and/or products in a manner that infringes at least Claims 1-20, 25, 27-28, 31-35, 37, 38, 41, 44, and 46 of the '250 patent.

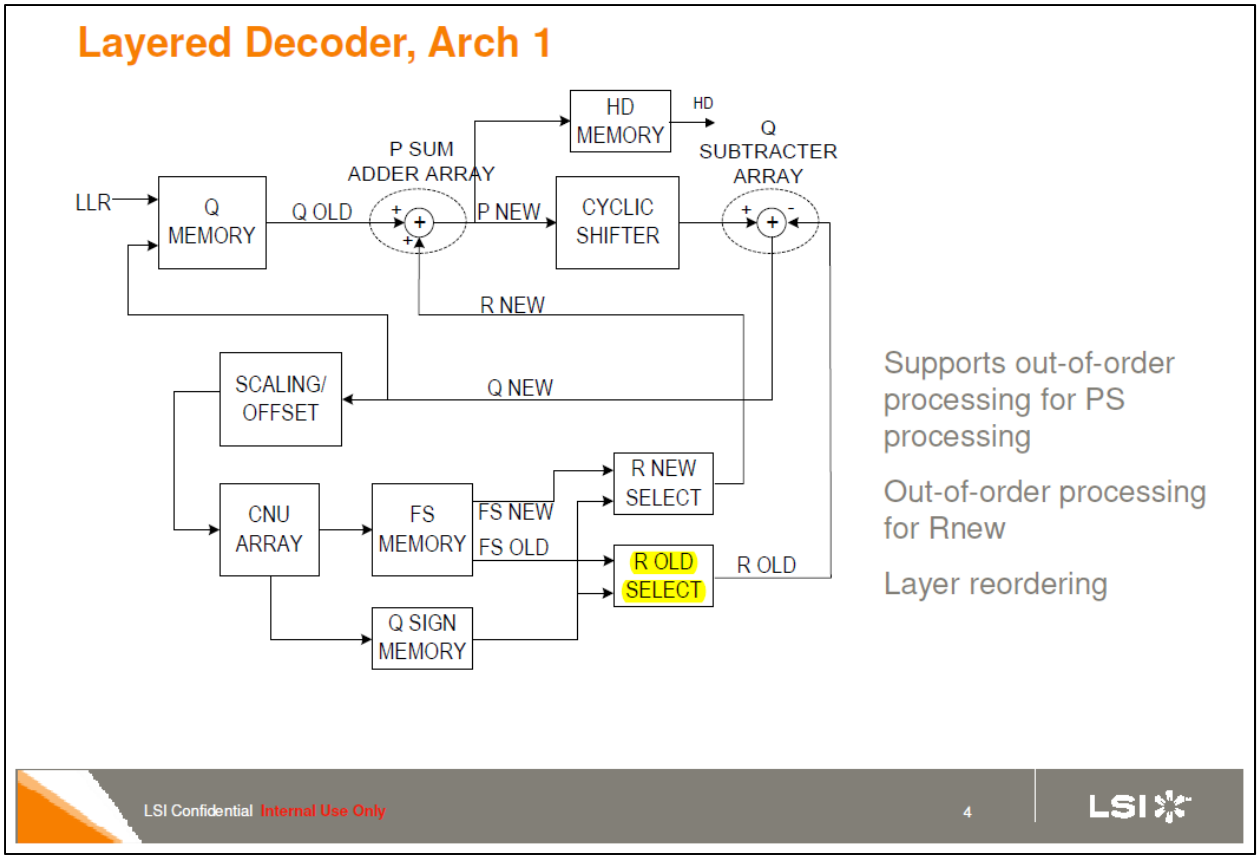
213. On information and belief, Defendant has directly infringed the '250 patent, for example, by making, using, selling, offering to sell, and/or importing into the United States the Accused Products, which meet each and every limitation of at least Claim 41 of the '250 patent, in violation of Plaintiff's patent rights and without Plaintiff's license or authority. Non-limiting examples of such infringement are provided below, based on the limited information currently available to Plaintiff.

214. Claim 1 of the '250 patent recites as follows:

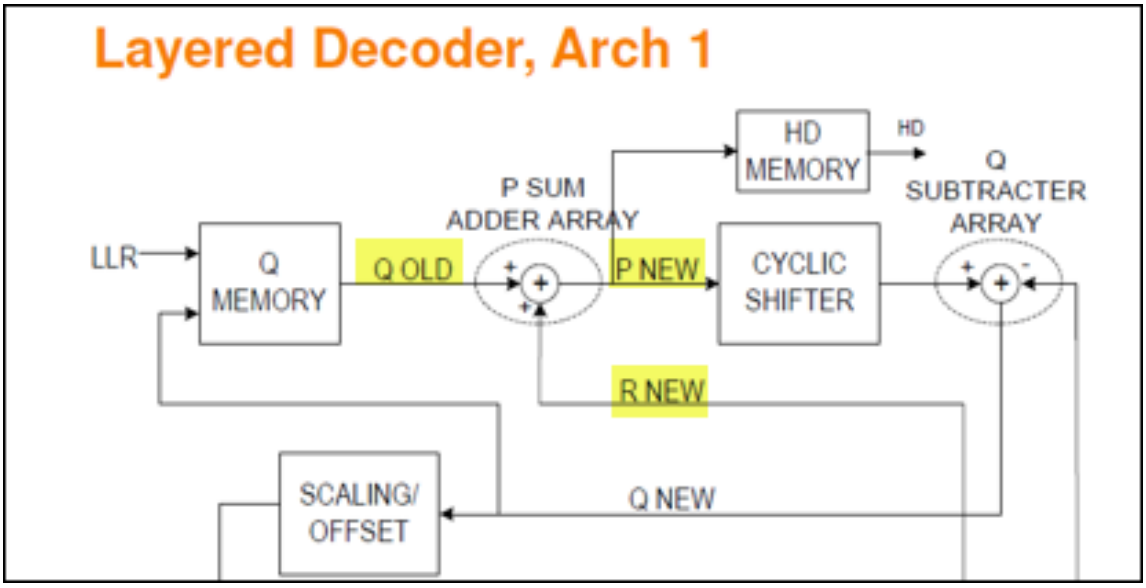
> A low density parity check (LDPC) code decoder, comprising:
> an R select unit that provides an R message by selecting from a plurality of possible R message values;
> a Q message memory that stores a Q message until an R message is generated by the R select unit, the Q message and the R message are combined to provide a P message; and
> a permuter that permutes the P message;
> wherein the permuter permutes the P message by the difference of the permutation of a block currently being processed and the permutation of a block previously processed; wherein the block currently being processed and the block previously processed are in a same block column.

215. On information and belief, the Accused Products satisfy each and every limitation of Claim 1. The Accused Products decode a low density parity check code. For example, the McLaren Architecture Presentation references the LDPC decoder, as set forth above.

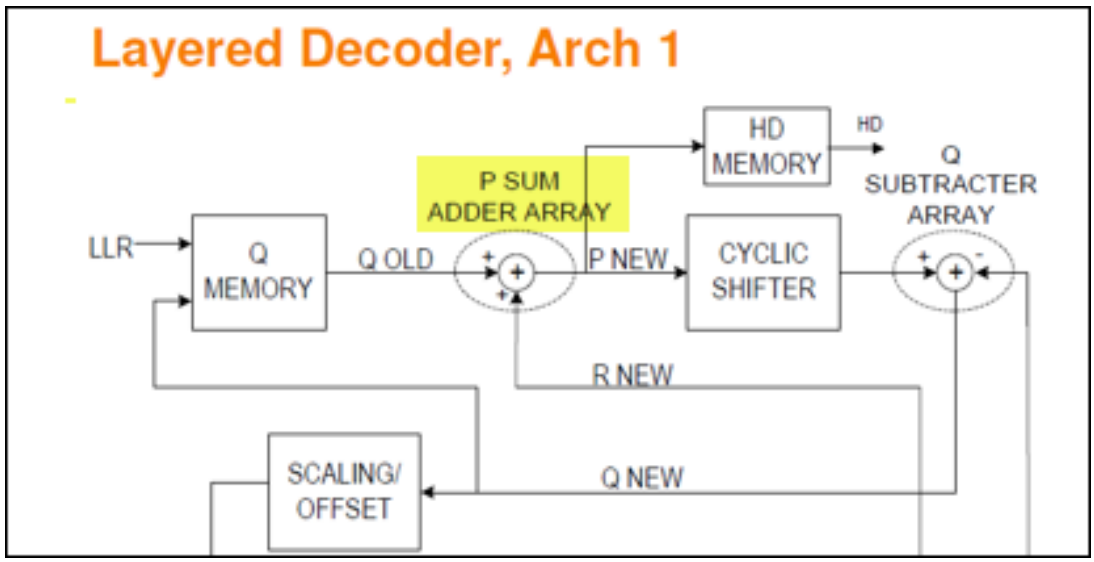
216. On information and belief, the Accused Products include an R select unit that provides an R message by selecting from a plurality of possible R message values. For example, the McLaren Architecture Presentation and the Layered Decoder Presentation each disclose the presence of an R NEW SELECT unit that selects a first R message from a plurality of previously generated possible R messages based on at least a message index value and a sign bit.



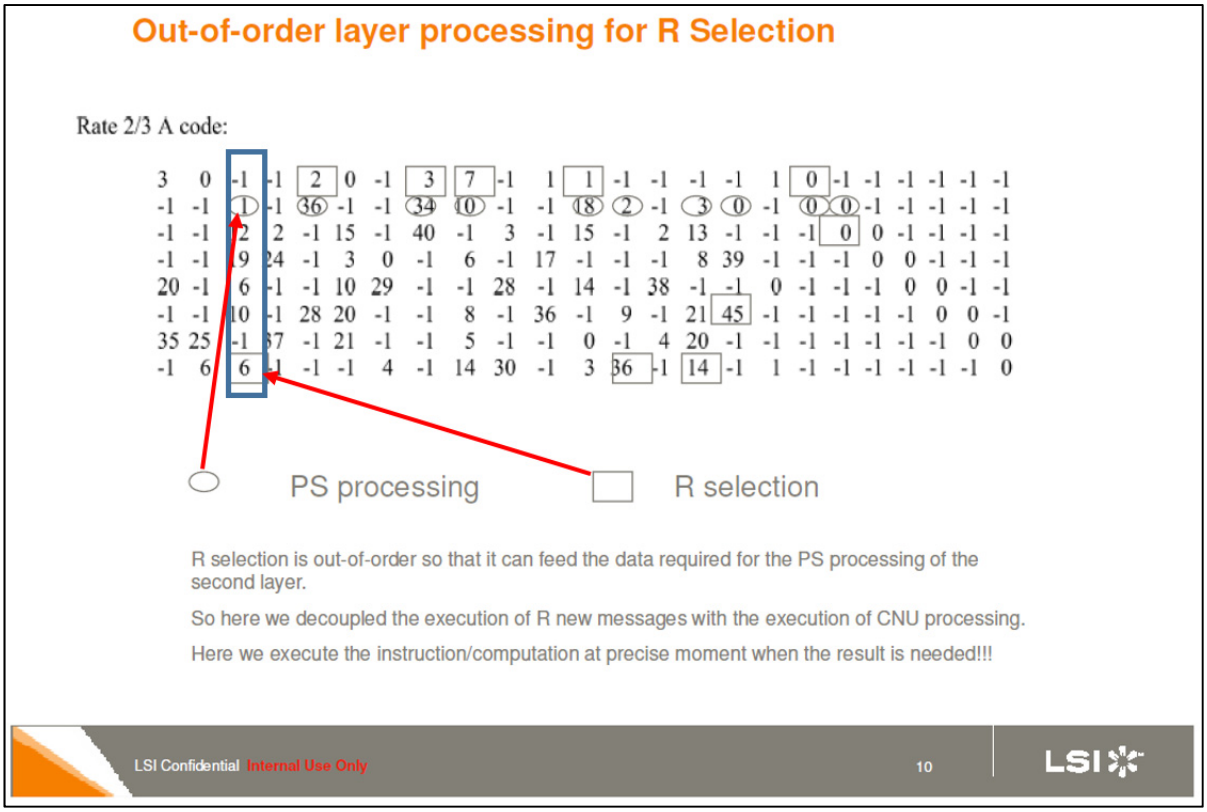
217. On information and belief, the Accused Products include a Q message memory (shown above) that stores a Q message until an R message is generated by the R select unit, the Q message and the R message are combined to provide a P message:



218. As shown below, the Accused Products also includes a permuter (i.e., a cyclic shifter) that permutes the P message:



219. The Accused Products include a permuter that permutes the P message by the difference of the permutation of a block currently being processed and the permutation of a block previously processed (*see* above); wherein the block currently being processed and the block previously processed are in a same block column (*see* below):

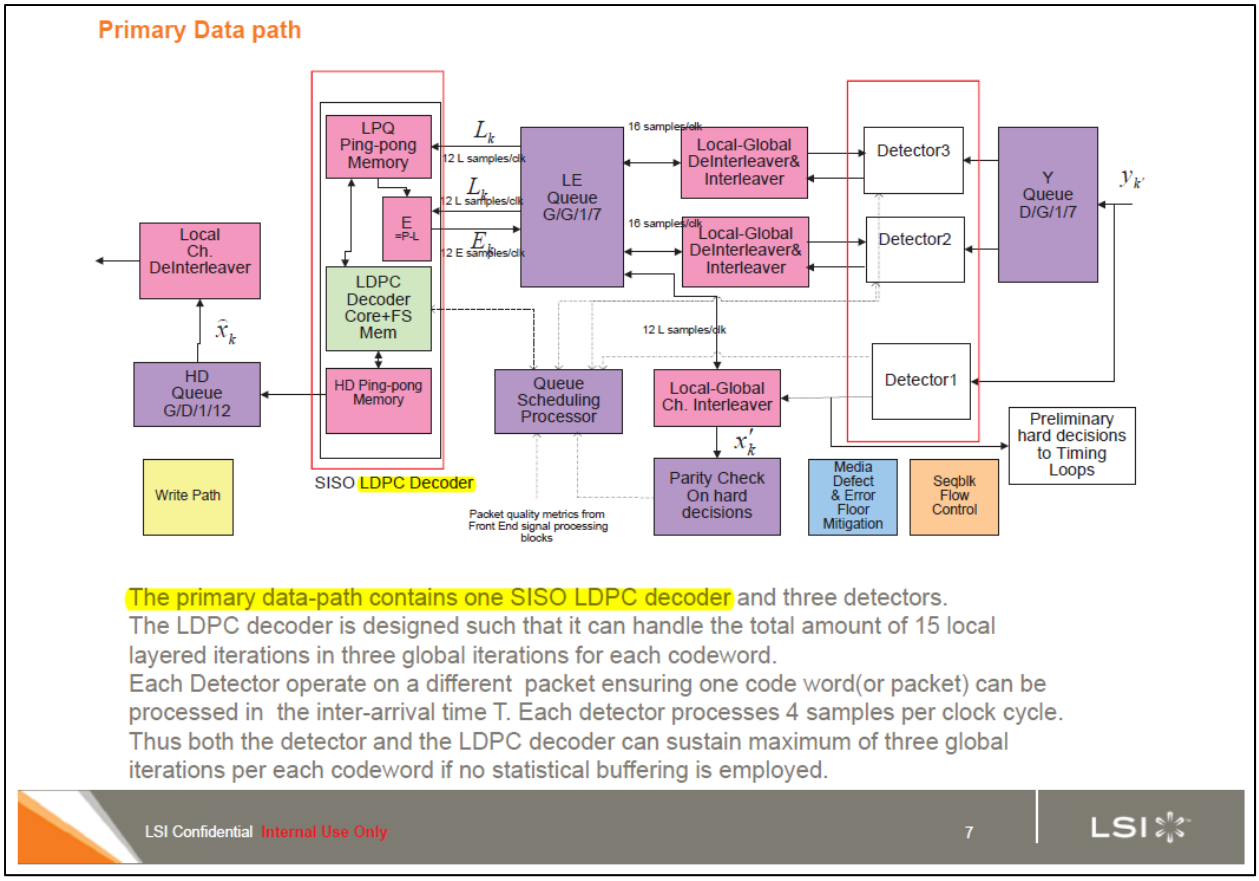


220. The method of claim 10 is practiced by the Accused Products for the same reasons set forth above with regard to the corresponding limitations of claim 1.

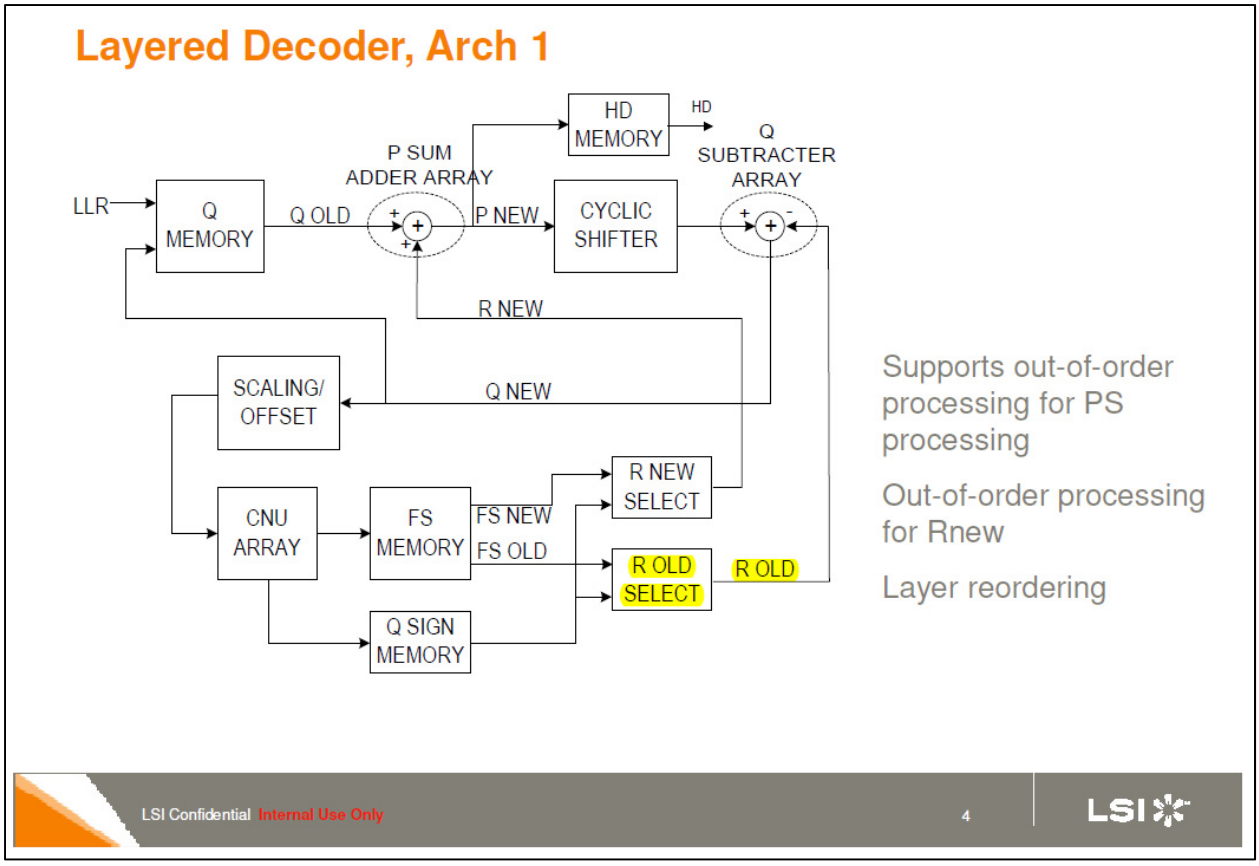
221. Claim 17 of the ’250 patent recites as follows:

> 17. A low density parity check (LDPC) code decoder, comprising:
> a first R select unit that provides an R message by selecting from a plurality of possible R message values,
> a Q message generator that combines the R message with a P message to produce a Q message; and
> a first permuter that permutes the P message;
> wherein the decoder is configured to update the P message based on determination of a final state for each block row.

222. On information and belief, the Accused Products satisfy each and every limitation of Claim 17. The Accused Products include an LDPC code decoder. For example, the McLaren Architecture Presentation references the LDPC decoder.

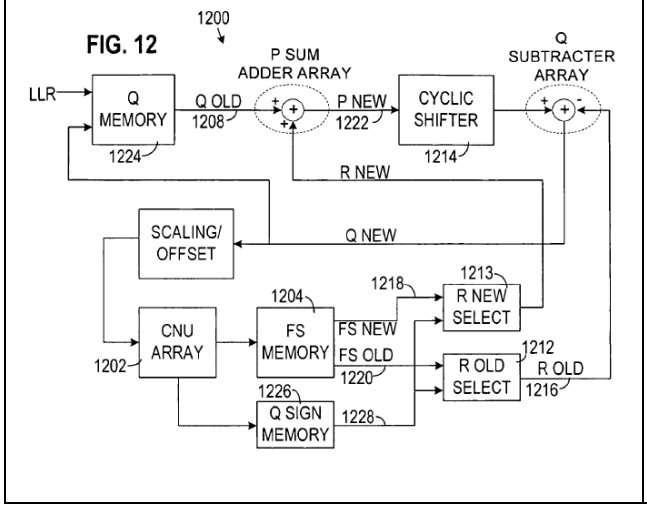


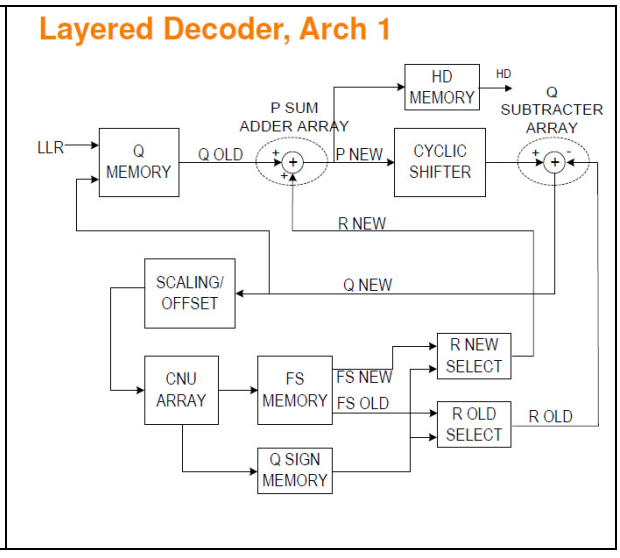
223. The Accused Products include a first R select unit that provides an R message by selecting from a plurality of possible R message values. For example, the Layered Decoder Presentation discloses the presence of an R OLD SELECT unit that provides an R message by selecting from a plurality of possible R message values.



224. The layered decoder architecture of the Accused Products is identical to what is set forth in the '250 patent.

'250 Patent at FIG. 12 | **Layered Decoder Presentation at 4**





225. The Accused Products include a Q message generator that combines the R message with a P message to produce a Q message. For example, the Layered Decoder Presentation discloses a Q SUBTRACTER ARRAY that combines the R message with a P message to produce a Q message.

For the irregular block LDPC codes, the TDMP algorithm can be described with equations (21)-(24):

$\vec{R}_{l,n}^{(0)} = 0, \vec{P}_n = \vec{L}_n^{(0)}$ [Initialization for each new received data frame], (21)

$\forall i = 1,2,\cdots,it_{\max}$ [Iteration loop],

$\forall l = 1,2,\cdots,j$ [Sub-iteration loop],

$\forall n = 1,2,\cdots,k$ [Block column loop],

$$\left[\vec{Q}_{l,n}^{(i)}\right]^{S(l,n)} = \left[\vec{P}_n\right]^{S(l,n)} - \vec{R}_{l,n}^{(i-1)}, \quad (22)$$

$$\vec{R}_{l,n}^{(i)} = f\left(\left[\vec{Q}_{l,n'}^{(i)}\right]^{S(l,n')}, \forall n' = 1,2,\cdots,k\right), \quad (23)$$

$$\left[\vec{P}_n\right]^{S(l,n)} = \left[\vec{Q}_{l,n}^{(i)}\right]^{S(l,n)} + \vec{R}_{l,n}^{(i)}, \quad (24)$$

where the vectors $\vec{R}_{l,n}^{(i)}$ and $\vec{Q}_{l,n}^{(i)}$ represent all the R and Q messages in each non-zero block of the H matrix, $s(l,n)$ denotes the shift coefficient for the l^{th} block row and n^{th} non-zero block of the H matrix (note that null blocks in the H matrix need not be processed); $\left[\vec{R}_{l,n}^{i-1}\right]^{S(l,n)}$ denotes that the vector $\vec{R}_{l,n}^{i-1}$ is cyclically shifted up by the amount $s(l,n)$, and k is the check-node degree of the block row or the layer. A negative sign on $s(l,n)$ indicates that it is cyclic down shift (equivalent cyclic left shift). $f(\cdot)$ denotes the check-node processing.

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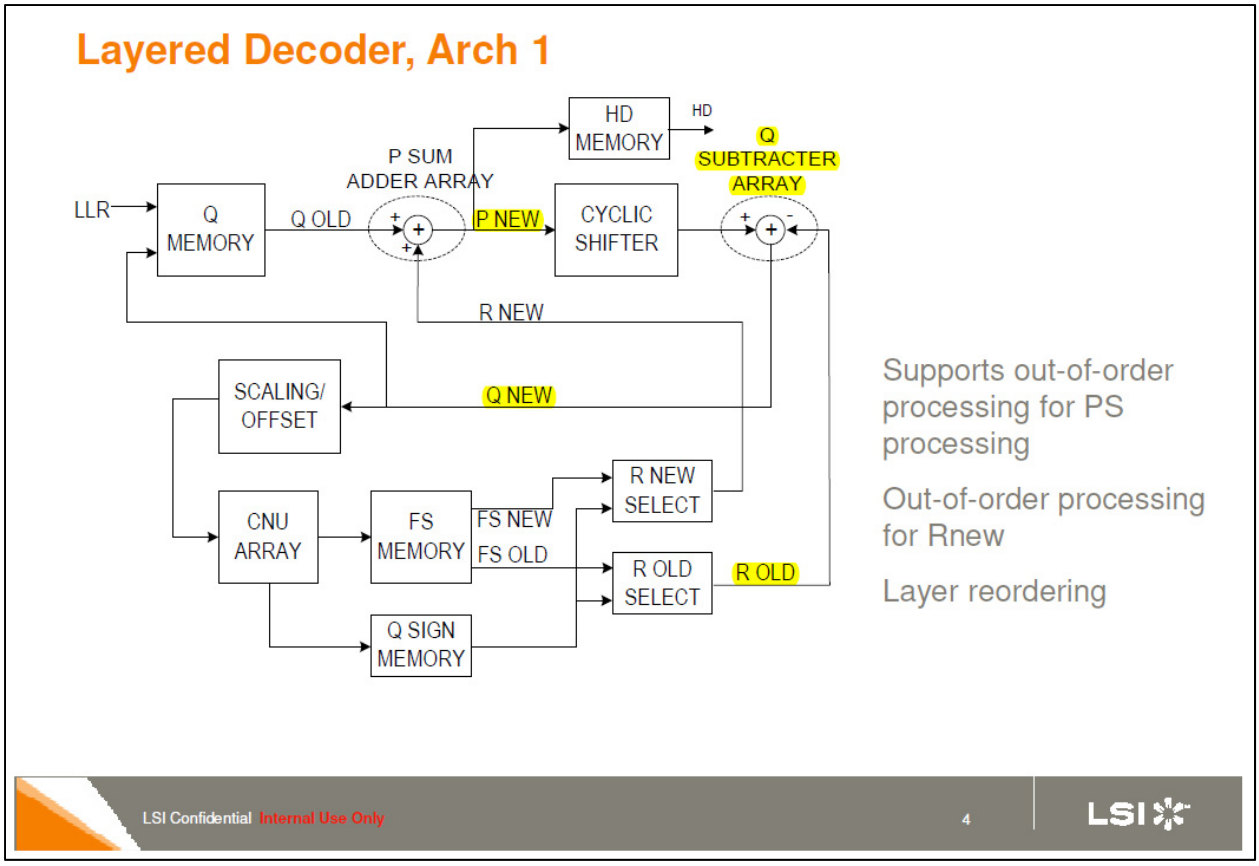


226. The TDMP algorithm equations of the Accused Products are identical to what is set forth in the '250 patent.

'250 Patent at 15:23–50

For the irregular block LDPC codes, the TDMP algorithm can be described with equations (21)-(24):

$\vec{R}_{l,n}^{(0)}=0, \vec{P}_n=\vec{L}_n^{(0)}$ [Initialization for each new received data frame],

$\forall i=1,2,\ldots,it_{max}$ [Iteration loop],

$\forall l=1,2,\ldots,j$ [Sub-iteration loop],

$\forall n=1,2,\ldots,k$ [Block column loop], (21)

$[\vec{Q}_{l,n}^{(i)}]^{S(l,n)}=[\vec{P}_n]^{S(l,n)}-\vec{R}_{l,n}^{(i-1)}$, (22)

$\vec{R}_{l,n}^{(i)}=f([\vec{Q}_{l,n}^{(i)}]^{S(l,n')}), \forall n'=1,2,\ldots,k)$, (23)

$[\vec{P}_n]^{S(l,n)}=[\vec{Q}_{l,n}^{(i)}]^{S(l,n)}+\vec{R}_{l,n}^{(i)}$, (24)

where the vectors $\vec{R}_{l,n}^{(i)}$ and $\vec{Q}_{l,n}^{(i)}$ represent all the R and Q messages in each non-zero block of the H matrix, s(l,n) denotes the shift coefficient for the l^{th} block row and n^{th} non-zero block of the H matrix (note that null blocks in the H matrix need not be processed); $[\vec{R}_{l,n}^{i-1}]^{S(l,n)}$ denotes that the vector $\vec{R}_{l,n}^{i-1}$ is cyclically shifted up by the amount s(l,n), and k is the check-node degree of the block row or the layer. A negative sign on s(l,n) indicates that it is cyclic down shift (equivalent cyclic left shift). f(•) denotes the check-node processing, which can be performed using BCJR, SP or MS.

Layered Decoder Presentation at 3

For the irregular block LDPC codes, the TDMP algorithm can be described with equations (21)-(24):

$\vec{R}_{l,n}^{(0)}=0, \vec{P}_n=\vec{L}_n^{(0)}$ [Initialization for each new received data frame], (21)

$\forall i=1,2,\cdots,it_{max}$ [Iteration loop],

$\forall l=1,2,\cdots,j$ [Sub-iteration loop],

$\forall n=1,2,\cdots,k$ [Block column loop],

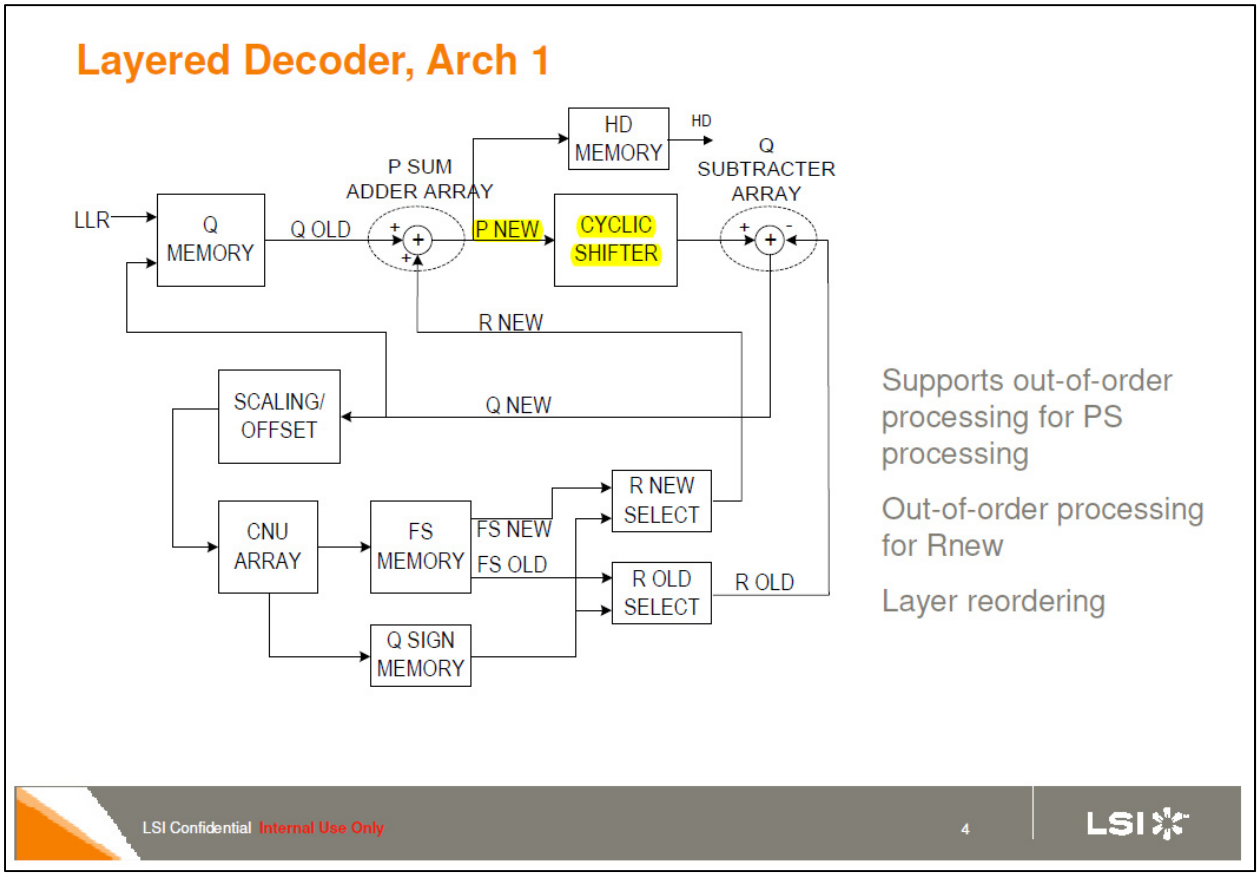
$\left[\vec{Q}_{l,n}^{(i)}\right]^{S(l,n)}=\left[\vec{P}_n\right]^{S(l,n)}-\vec{R}_{l,n}^{(i-1)}$, (22)

$\vec{R}_{l,n}^{(i)}=f\left(\left[\vec{Q}_{l,n}^{(i)}\right]^{S(l,n')}, \forall n'=1,2,\cdots,k\right)$, (23)

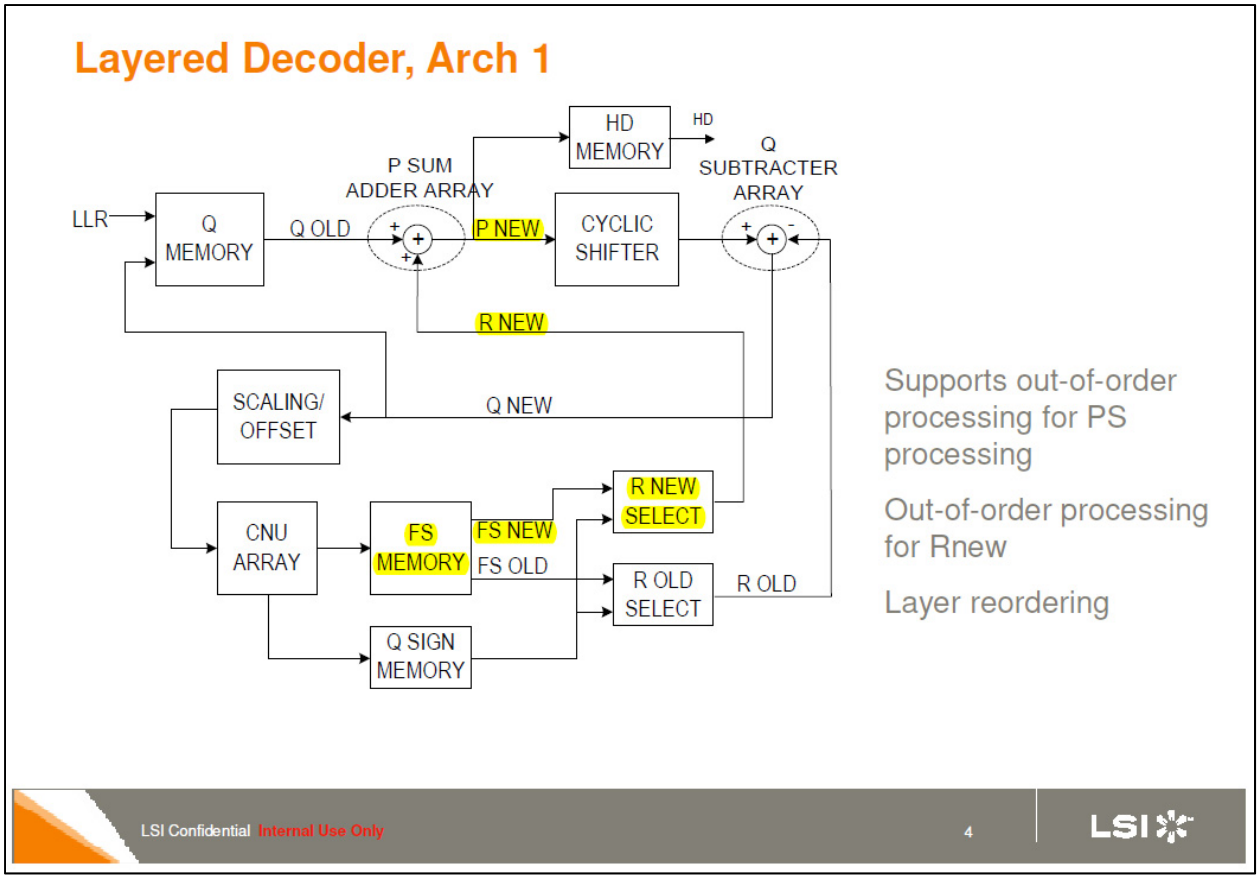
$\left[\vec{P}_n\right]^{S(l,n)}=\left[\vec{Q}_{l,n}^{(i)}\right]^{S(l,n)}+\vec{R}_{l,n}^{(i)}$, (24)

where the vectors $\vec{R}_{l,n}^{(i)}$ and $\vec{Q}_{l,n}^{(i)}$ represent all the R and Q messages in each non-zero block of the H matrix, $s(l,n)$ denotes the shift coefficient for the l^{th} block row and n^{th} non-zero block of the H matrix (note that null blocks in the H matrix need not be processed); $\left[\vec{R}_{l,n}^{i-1}\right]^{S(l,n)}$ denotes that the vector $\vec{R}_{l,n}^{i-1}$ is cyclically shifted up by the amount $s(l,n)$, and k is the check-node degree of the block row or the layer. A negative sign on $s(l,n)$ indicates that it is cyclic down shift (equivalent cyclic left shift). $f(\cdot)$ denotes the check-node processing.

227. The Accused Products include a first permuter that permutes the P message. For example, the Layered Decoder Presentation discloses a CYCLIC SHIFTER that permutes the P message.



228. The Accused Products include wherein the decoder is configured to update the P message based on determination of a final state for each block row. For example, the Layered Decoder Presentation discloses that the P message is a function of R NEW, and R NEW is based on a determination of a final state for each block row.



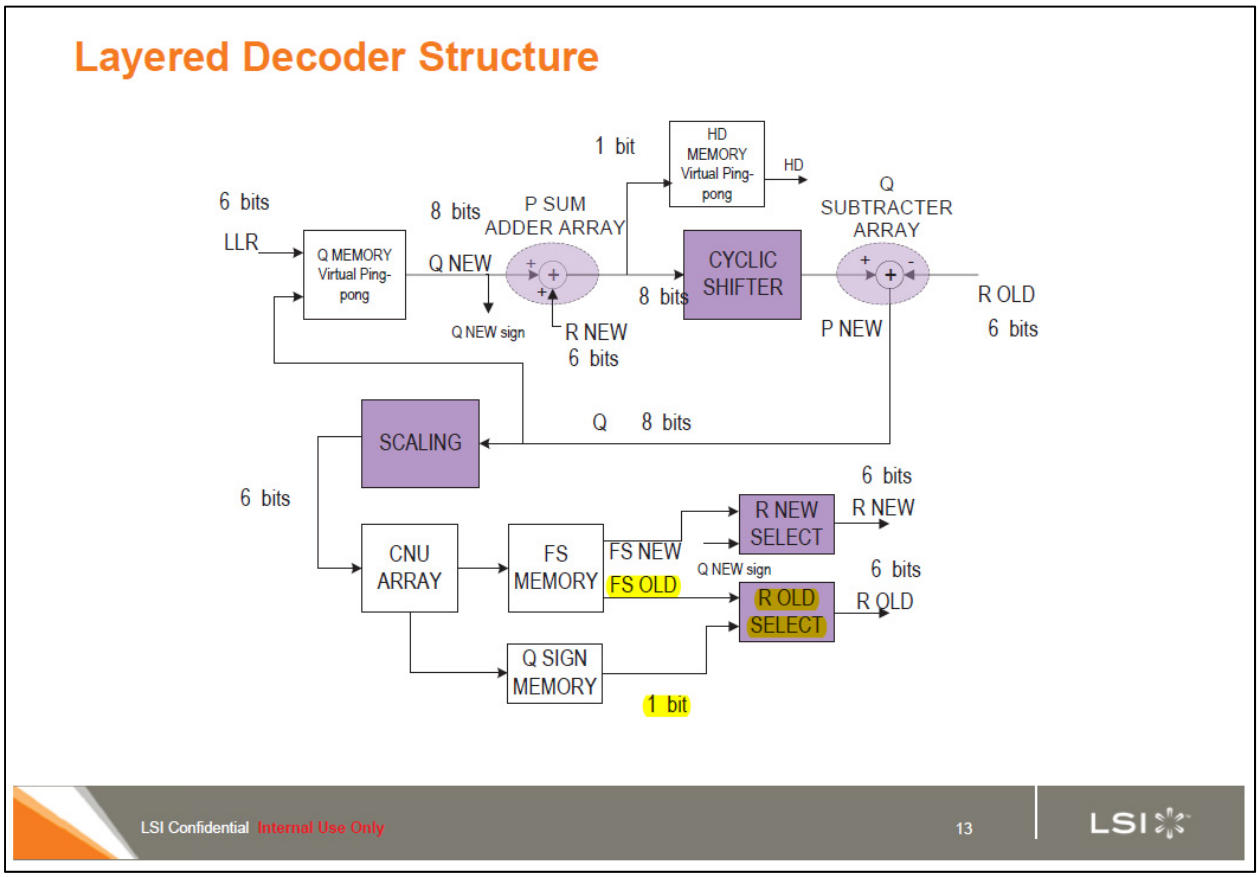
229. Claim 32 of the '250 patent recites as follows:

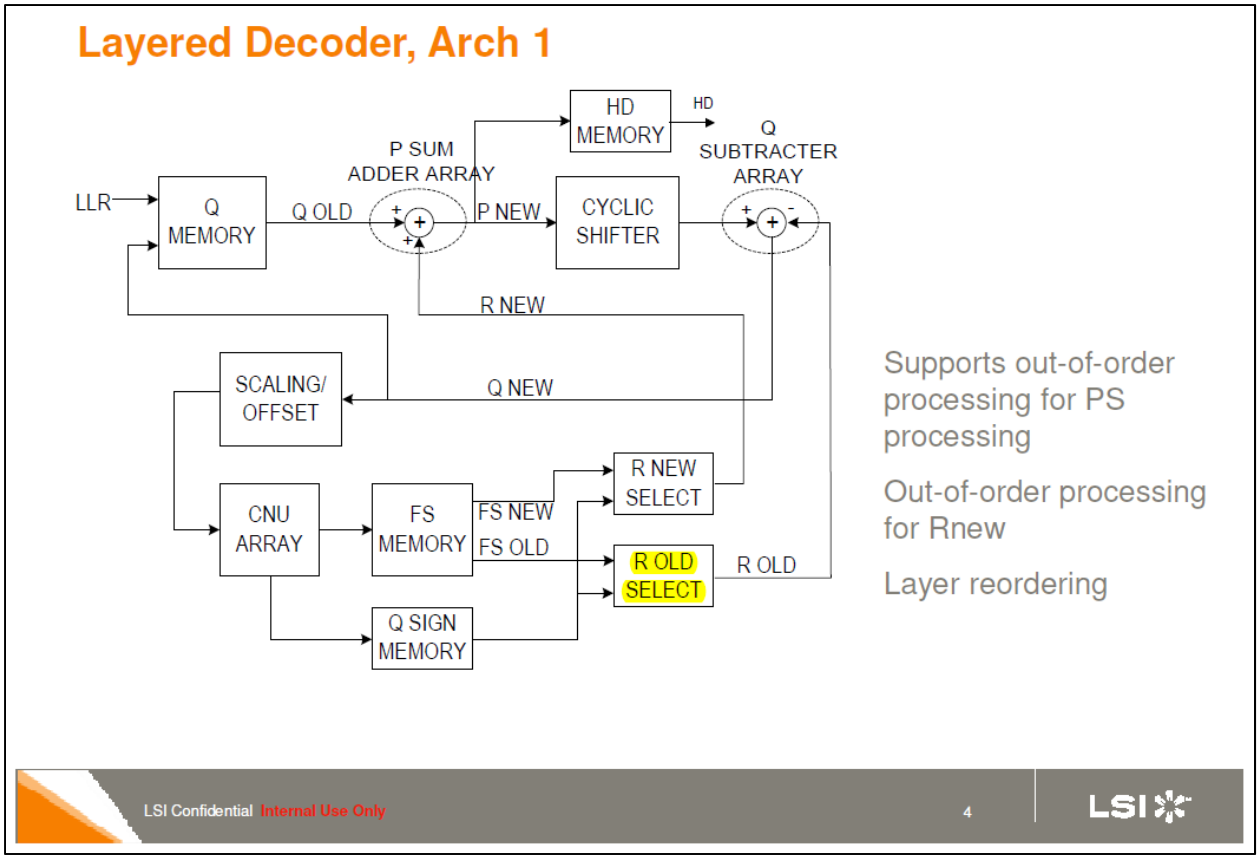
> 32. A method for decoding a low density parity check code, comprising:
> selecting a first R message from a plurality of previously generated possible R messages based on at least a message index value and a sign bit;
> generating a Q message by combining the first R message with a P message;
> permuting the P message; and
> updating the P message responsive to determination of a final state for each block row.

230. On information and belief, the Accused Products satisfy each and every limitation of Claim 32. The Accused Products decode an LDPC code. *See* ¶ 225, 91, *supra*.

231. The Accused Products select a first R message from a plurality of previously generated possible R messages based on at least a message index value and a sign bit. For

example, the McLaren Architecture Presentation and the Layered Decoder Presentation each disclose the presence of an R OLD SELECT unit that selects a first R message from a plurality of previously generated possible R messages based on at least a message index value and a sign bit.





232. The Accused Products generate a Q message by combining the first R message with a P message. *See* ¶ 225, 191, 91, *supra*.

233. The Accused Products permute the P message. *See* ¶ 140, *supra*.

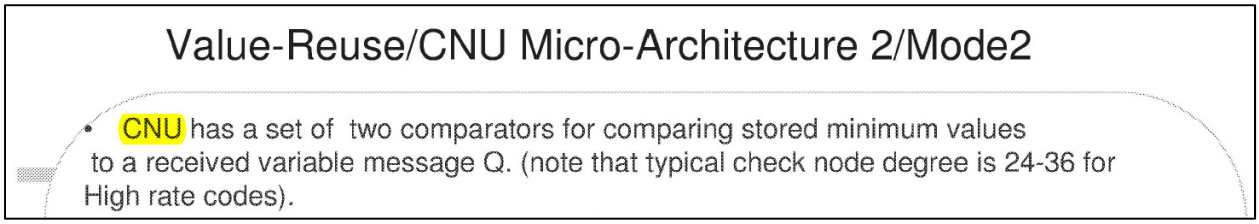
234. The Accused Products update the P message responsive to determination of a final state for each block row. *See* ¶ 225, 194, 91, *supra*.

235. Claim 41 of the '250 patent recites as follows:

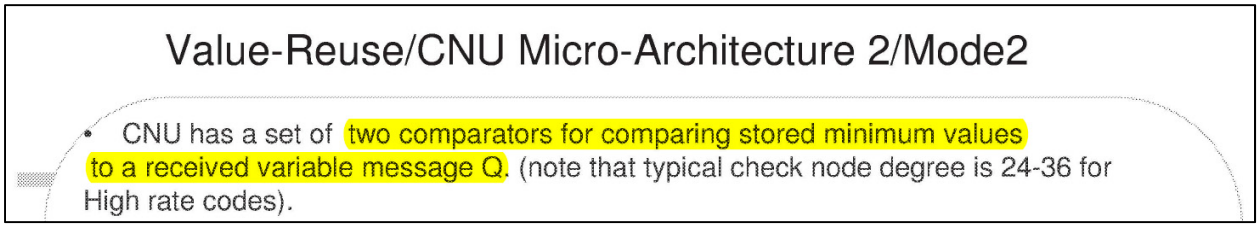
> 41. A low density parity check code decoder, comprising:
> a check node unit (CNU); the CNU comprising:
> a set of comparators for comparing stored minimum values to a received variable message Q, wherein:
> a total number of comparators in the set is less than the check node degree;
> a first comparator of the set determines a first minimum value, M1, by comparing a first stored minimum value, $M1_{PS}$, and the received variable message Q; and
> a second comparator of the set determines a second minimum value, M2, by comparing a second stored minimum value, $M2_{PS}$, and the received variable message Q; and
> final state storage that stores:
> $M1_{PS}$, and
> $M2_{PS}$; and
> a computation unit that computes a message transferred from the check node to a variable node based on the values of $M1_{PS}$ and $M2_{PS}$ stored in the final state storage.

236. On information and belief, the Accused Products satisfy each and every limitation of Claim 41. The Accused Products include a low density parity check code decoder. For example, the McLaren Architecture Presentation references the LDPC decoder. *See* ¶ 128, 231, *supra*.

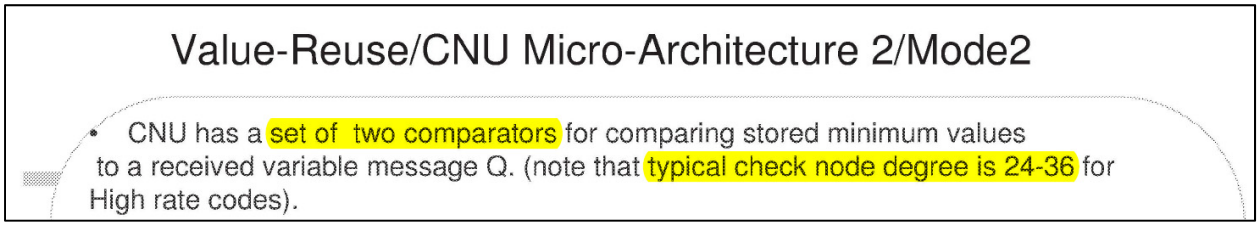
237. The Accused Products include a check node unit (CNU). For example, a presentation given by LSI engineers at the 42nd Asilomar Conference on Signals, Systems, and Computers on October 28, 2008 is titled "Next Generation Iterative LDPC Solutions for Magnetic Recording Storage" (hereinafter, the "Asilomar Presentation") and discloses a check node unit.



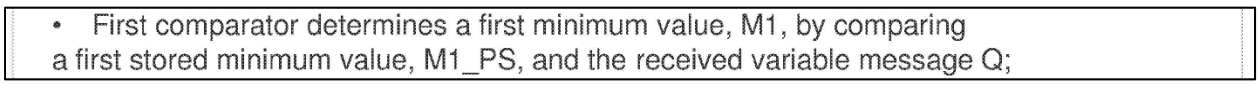
238. The Accused Products include a set of comparators for comparing stored minimum values to a received variable message Q. For example, the "Asilomar Presentation" discloses a check node unit.



239. The Accused Products include wherein a total number of comparators in the set is less than the check node degree. For example, the Asilomar Presentation discloses that the total number of comparators in the set is two, which is less than the disclosed typical check node degree of 24-36.



240. The Accused Products include wherein a first comparator of the set determines a first minimum value, M1, by comparing a first stored minimum value, $M1_{PS}$, and the received variable message Q. For example, the Asilomar Presentation discloses that a first comparator determines a first minimum value, M1, by comparing a first stored minimum value, M1_PS, and the received variable message Q.



241. The Accused Products include wherein a second comparator of the set determines a second minimum value, M2, by comparing a second stored minimum value, $M2_{PS}$, and the received variable message Q. For example, the Asilomar Presentation discloses that a second

comparator determines a second minimum value, M2, by comparing a second stored minimum value, M2_PS, and the received variable message Q.

- Second comparator determines a second minimum value, M2, by comparing a second stored minimum value, M2_PS, and the received variable message Q;

242. The Accused Products include final state storage that stores $M1_{PS}$, and $M2_{PS}$. For example, the Asilomar Presentation discloses that final state storage stores M1_PS and M2_PS.

- Final state storage stores: M1_PS and M2_PS.

243. The Accused Products include a computation unit that computes a message transferred from the check node to a variable node based on the values of $M1_{PS}$ and $M2_{PS}$ stored in the final state storage. For example, the Asilomar Presentation discloses that the R Select Unit computes R messages based on the values of M1_PS and M2_PS stored in the final state storage.

- R Select Unit computes R messages based on the values of M1_PS and M2_PS stored in the final state storage.

244. In view of the foregoing, the Accused Products directly infringe at least Claims 1-20, 25, 27-28, 31-35, 37, 38, 41, 44, and 46 of the '250 patent at least through Defendant's and/or Broadcom Predecessor Entities' sale, offer for sale, importation, use, and/or testing of the Accused Products.

245. On information and belief, Defendant and/or Broadcom Predecessor Entities should have known that they directly infringe as of the date LSI became aware of the issuance of the '250 patent, and in any event no later than the date LSI was advised of the issuance of impending issuance the '250 patent by Dr. Gunnam on January 31, 2014, and in any event on or about February 18, 2014 when the '250 patent issued.

246. Defendant further has knowledge of the ’250 patent at least as early as the filing and/or service of this Complaint. Defendant is further aware that the Accused Products necessarily practice Claims 1-20, 25, 27-28, 31-35, 37, 38, 41, 44, and 46 of the ’250 patent.

247. On information and belief, Defendant takes active steps to induce infringement by others of at least Claims 1-20, 25, 27-28, 31-35, 37, 38, 41, 44, and 46 of the ’250 patent in violation of 35 U.S.C. §271(b), including, for example, by (a) inducing manufacturers to perform the claimed inventions when testing the Accused Products, and (b) inducing end users to perform the claimed inventions when using the Accused Products. Such active steps include, but are not limited to, selling Accused Products with the knowledge and intent that the Accused Products will be operated by such manufacturers and their customers in accordance with the claimed inventions.

248. On information and belief, Defendant and/or Broadcom Predecessor Entities knew or should have known that such activities induce others to directly infringe one or more of at least Claims 1-20, 25, 27-28, 31-35, 37, 38, 41, 44, and 46 of the ’250 patent. For example, Defendant and/or Broadcom Predecessor Entities should have known that their actions induced others to directly infringe as of the date LSI became aware of the issuance of the ’250 patent no later than the date LSI was advised of the issuance of impending issuance the ’250 patent by Dr. Gunnam on January 31, 2014, and in any event on or about February 18, 2014 when the ’250 patent issued. Defendant and/or Broadcom Predecessor Entities were further informed that the technology in the Accused Products infringed the ’250 patent, and Defendant and/or Broadcom Predecessor Entities knowingly and purposefully continued to exploit the patented technology despite knowing that it was covered by the ’250 patent.

249. On information and belief, Defendant and/or Broadcom Predecessor Entities have contributed to the infringement of at least Claims 1-20, 25, 27-28, 31-35, 37, 38, 41, 44, and 46 of the '250 patent by others, including consumer/end-user use of the Accused Products, in violation of 35 U.S.C. § 271(c). Acts by Defendant and/or Broadcom Predecessor Entities that contribute to the infringement of others include, but are not limited to, the sale, offer for sale, and/or import by Defendant of the Accused Products. Such Accused Products are especially made for or adapted for use to infringe, and are not a staple article of commerce and are not suitable for substantial non-infringing use. The Accused Products are apparatuses for use in practicing Claims 1-20, 25, 27-28, 31-35, 37, 38, 41, 44, and 46 of the '250 patent and are at least a material part of those claimed inventions, for example, as described above with respect to Claim 1. As also described above, Defendant has, on information and belief, been on notice of the '250 patent since it issued on February 18, 2014, and in addition since filing and/or service of this Complaint, and defendant has further been aware that use of the Accused Products necessarily practice Claims 1-20, 25, 27-28, 31-35, 37, 38, 41, 44, and 46 of the '250 patent.

250. The Accused Products are especially made for or adapted for use to infringe, and are not a staple article of commerce and are not suitable for substantial non-infringing use. By way of example, the use of the LDPC decoders included in the Accused Products is necessary to use the accused products for their intended purpose (decoding data from a hard disk drive, solid state drive, or wireless digital transmission), and the LDPC decoders necessarily perform the claimed inventions when they decode data. Accordingly, the Accused Products do not have a substantial use that does not entail practicing the claimed inventions. On information and belief, the Accused Products cannot be used but to infringe the '250 patent.

251. Despite Defendant's knowledge, notice, and infringement of the '250 patent, Defendant continues to manufacture, use, sell, offer for sale, and/or import the Accused Products in a manner that willfully infringes the '250 patent, and on information and belief continues to sell and/or offer for sale the Accused Products to the United States market. Defendant's infringement of the '250 patent is willful, as set forth above. Defendant lacks a justifiable belief that it does not infringe the '250 patent, or that the '250 patent is invalid or unenforceable, and has acted recklessly in its infringing activity, justifying an increase in the damages to be awarded to Plaintiff up to three times the amount found or assessed, in accordance with 35 U.S.C. § 284.

252. On information and belief, Defendant had actual or constructive knowledge of the '250 patent since at least February 18, 2014.

253. Defendant further has knowledge of the '250 patent at least as early as the filing and/or service of this Complaint. Defendant knows or should know as of the date of filing and/or service of the Complaint that its actions induced others to directly infringe the '250 patent and contributed to infringement of the '250 patent.

254. This case is rendered an exceptional case at least in light of Defendant's willful infringement of the '250 patent, justifying an award to Plaintiff of its reasonable attorney fees, in accordance with 35 U.S.C. § 285.

255. Defendant has no adequate remedy at law for Defendant's acts of infringement. As a direct and proximate result of Defendant's acts of infringement, Plaintiff has suffered and continues to suffer damages and irreparable harm. Unless Defendant's acts of infringement are enjoined by this Court, Plaintiff will continue to be damaged and irreparably harmed.

256. Defendant's infringement of the '250 patent has damaged and continues to damage Plaintiff in an amount yet to be determined, of at least a reasonable royalty and/or lost profits that Plaintiff would have made but for Defendant's infringement acts.

COUNT VI
(Infringement under 35 U.S.C. § 271 of U.S. Patent No. 10,141,950)

257. Plaintiff repeats and re-alleges the paragraphs above as if fully set forth herein.

258. The '950 patent is valid, enforceable, and was duly issued on November 27, 2018 in full compliance with Title 35 of the United States Code.

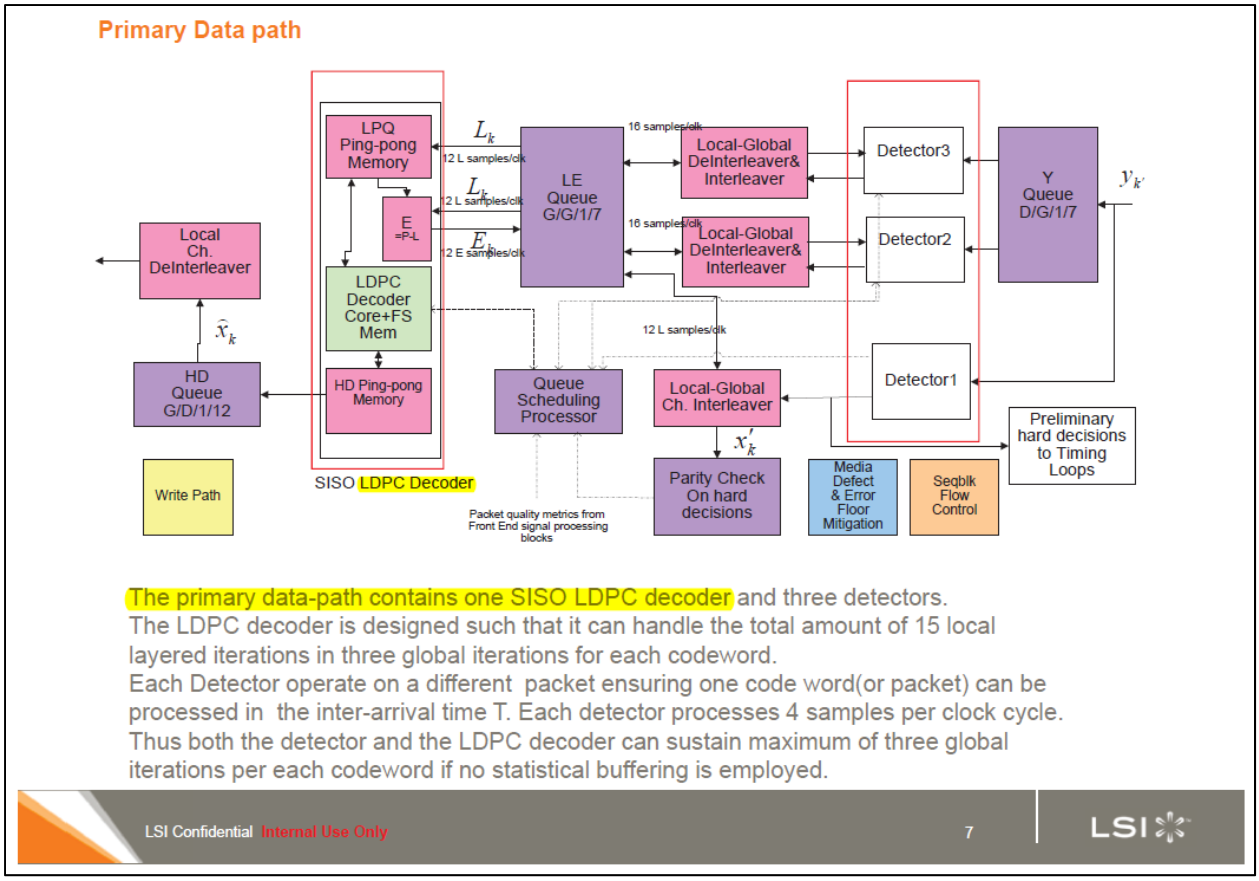
259. On information and belief, in violation of 35 U.S.C. § 271, Defendant has infringed, contributed to the infringement of, and/or induced others to infringe the '950 patent, either literally or under the doctrine of equivalents, by, among other things, making, using, offering for sale, selling, and/or importing into the United States unlicensed systems and/or products in a manner that infringes at least Claims 1-16 of the '950 patent.

260. On information and belief, Defendant has directly infringed the '950 patent, for example, by making, using, selling, offering to sell, and/or importing into the United States the Accused Products, which meet each and every limitation of at least Claim 1 of the '950 patent, in violation of Plaintiff's patent rights and without Plaintiff's license or authority. Non-limiting examples of such infringement are provided below, based on the limited information currently available to Plaintiff.

261. Claim 1 of the ’950 patent recites as follows:

> 1. A low density parity check (LDPC) code decoder, comprising:
> decoding circuitry configured to process blocks of an LDPC matrix, the decoding circuitry comprising:
> a control unit that controls processing by the decoding circuitry, the control unit configured to cause the decoding circuitry to process blocks of a layer of the LDPC matrix out of order, wherein the control unit is configured to cause the decoding circuitry to process each block of the LDPC matrix in processing substeps comprising:
> an R new update substep that provides an R new message, wherein the R new message is produced for a block of a different layer of the matrix from a layer containing a block currently being processed;
> an R old update substep that selects an R old message, wherein the R old message is produced for a layer of the matrix currently being processed;
> a P message substep that generates updated P messages;
> a Q message substep that computes variable node messages (Q messages); and
> a partial state substep that updates partial state of a block row based on Q messages computed for the block (check node unit (CNU) Partial state processing).

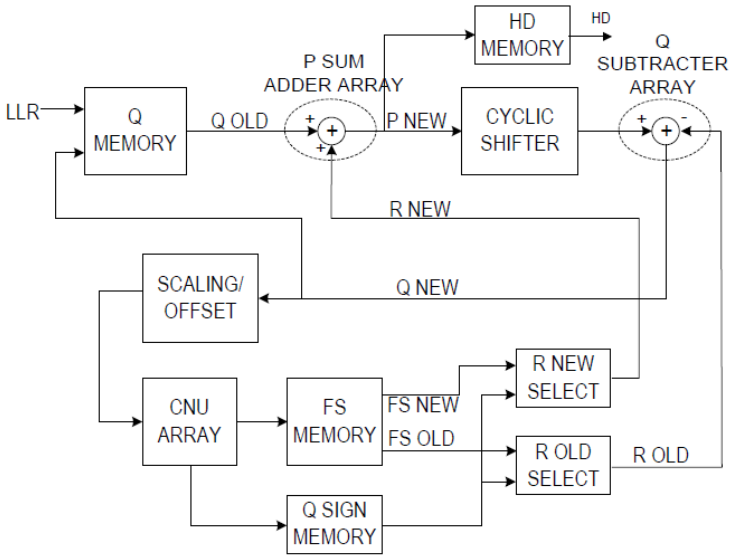
262. On information and belief, the Accused Products satisfy each and every limitation of Claim 1. The Accused Products comprise an LDPC code decoder. For example, the McLaren Architecture Presentation references the LDPC decoder.



263. The Accused Products include decoding circuitry, and as set forth below, that decoding circuitry is configured to process blocks of an LDPC matrix.

264. The Accused Products include a control unit that controls processing by the decoding circuitry, the control unit configured to cause the decoding circuitry to process blocks of a layer of the LDPC matrix out of order. For example, the Layered Decoder Presentation references out of order processing and includes many figures taken directly from the ’950 patent.

Layered Decoder, Arch 1

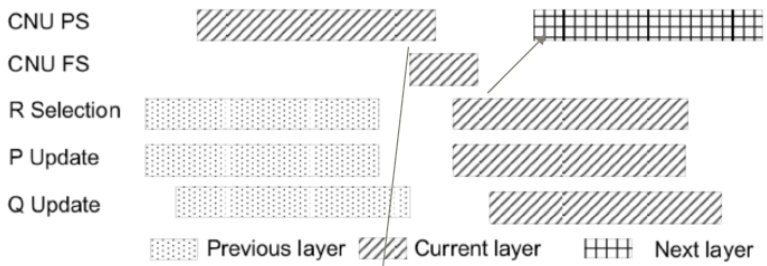


Supports out-of-order processing for PS processing

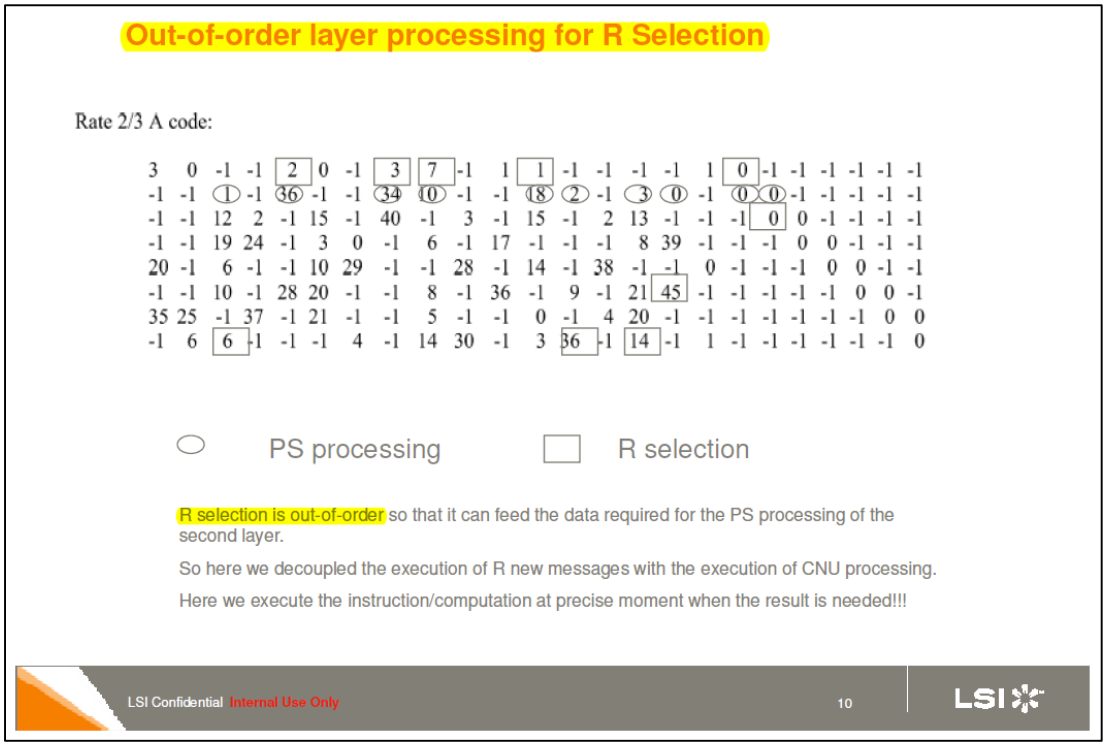
Out-of-order processing for Rnew

Layer reordering

Out-of-order processing for PS processing

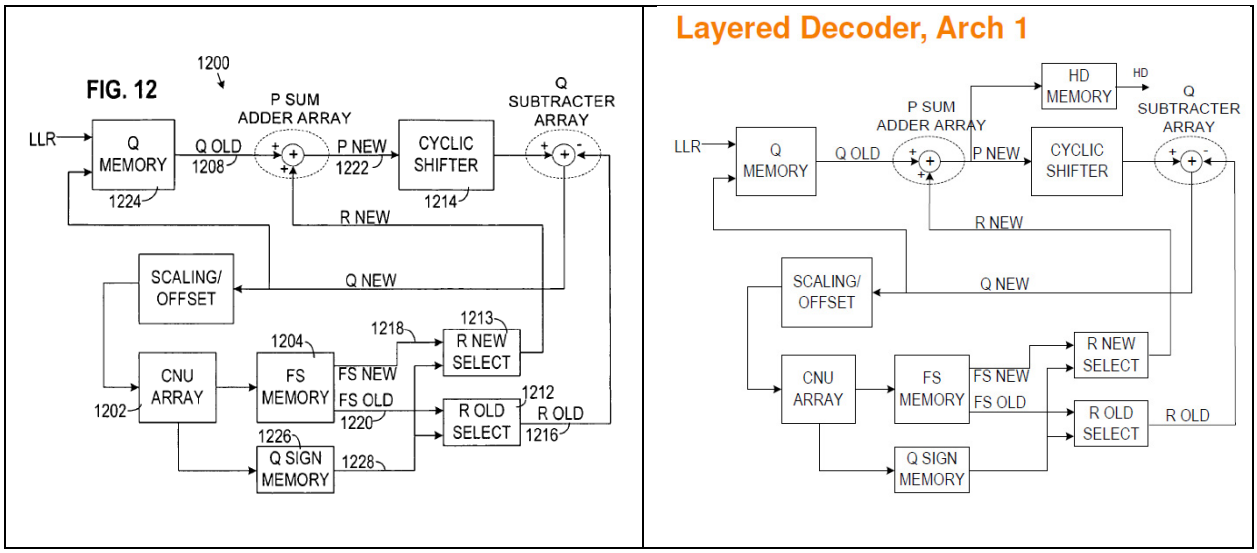


The circulants in each layers can be processed out-of-order

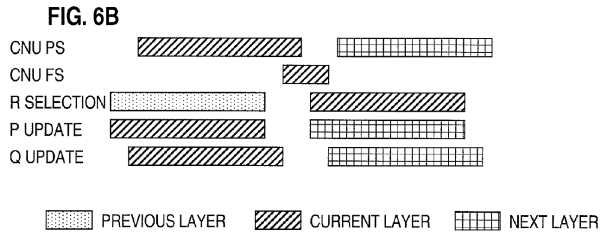
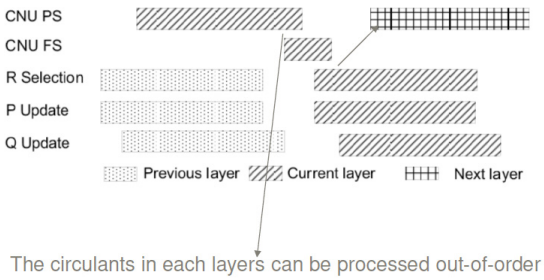


265. The layered decoder architecture of the Accused Products is identical to what is set forth in the '950 patent.

'950 Patent at FIG. 12 **Layered Decoder Presentation at 4**

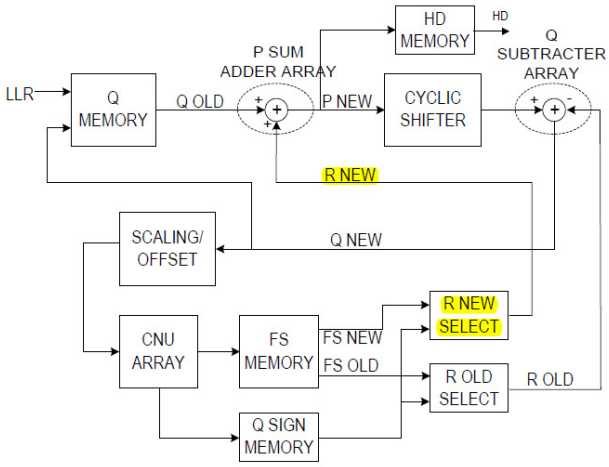


266. The pipeline architecture of the Accused Products is similar to what is set forth in the ’950 patent.

’950 Patent at FIG. 6B	**Layered Decoder Presentation at 8**
	

267. The Accused Products include a control unit configured to cause the decoding circuitry to process each block of the LDPC matrix in processing substeps comprising an R new update substep that provides an R new message, wherein the R new message is produced for a block of a different layer of the matrix from a layer containing a block currently being processed. For example, the Layered Decoder Presentation discloses an R NEW SELECT unit that produces an R new message for a block of a different layer of the matrix from a layer containing a block currently being processed.

Layered Decoder, Arch 1

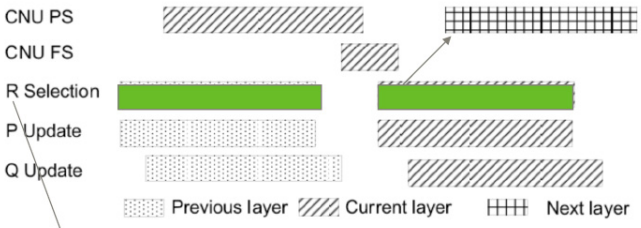


Supports out-of-order processing for PS processing

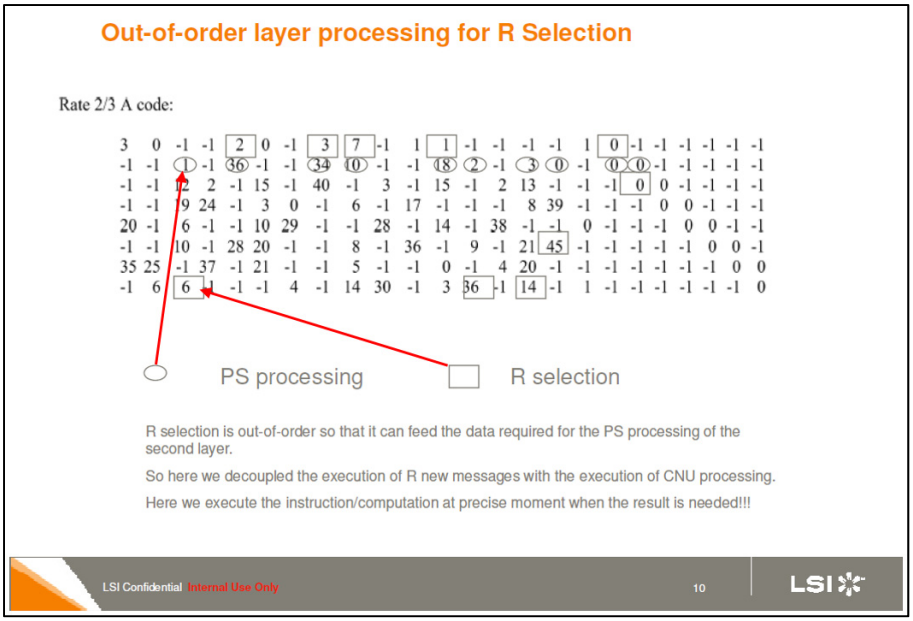
Out-of-order processing for Rnew

Layer reordering

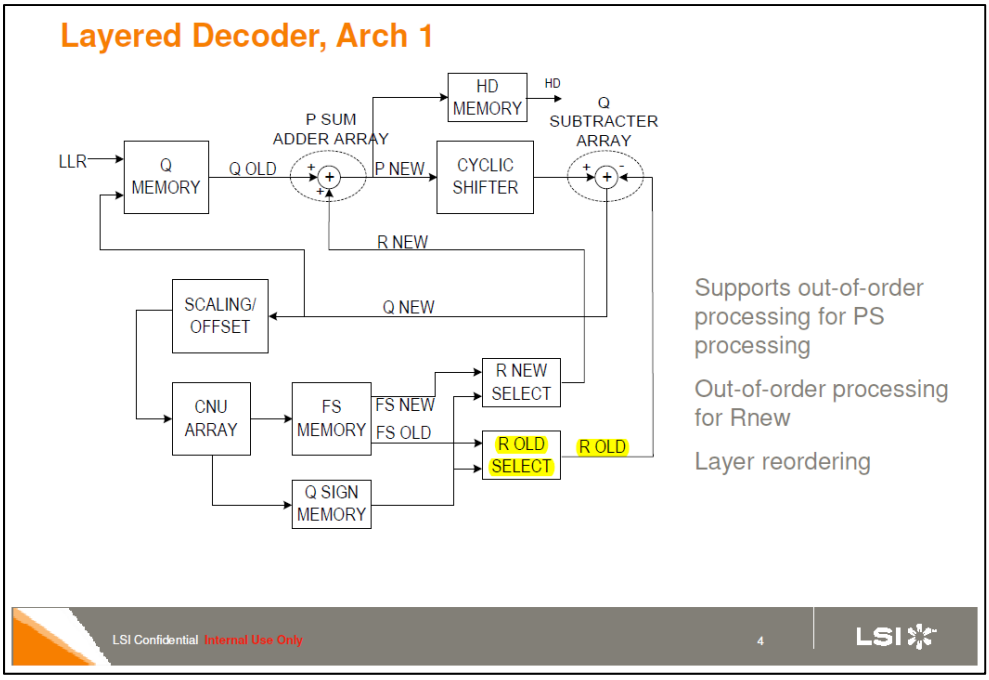
Out-of-order processing of R_{new}



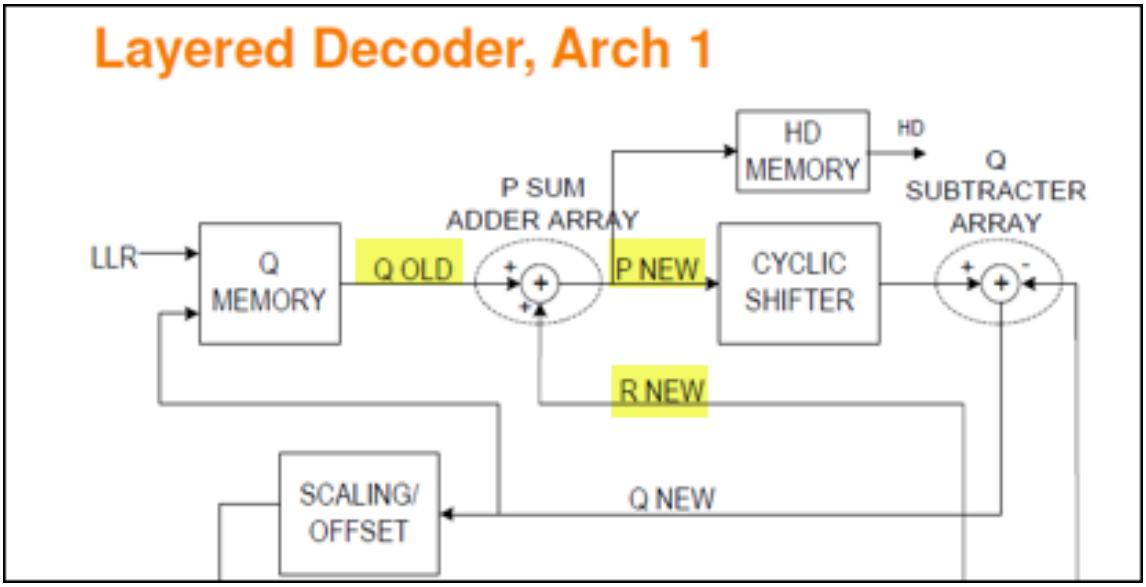
R selection for R_{new} operates out-of-order to feed the data for PS processing of next layer



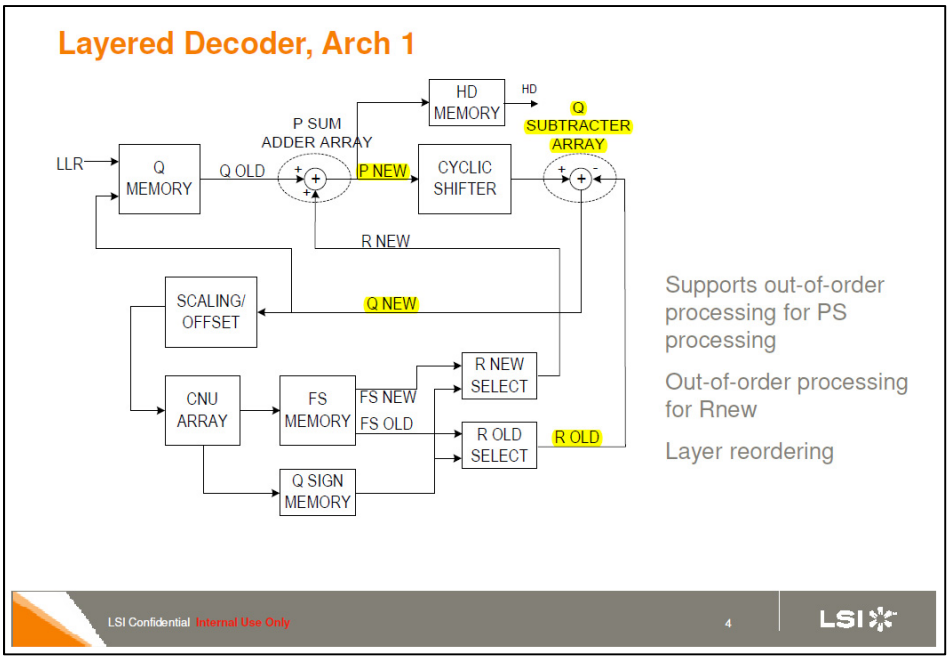
268. The Accused Products include a control unit configured to cause the decoding circuitry to process each block of the LDPC matrix in processing substeps comprising an R old update substep that selects an R old message, wherein the R old message is produced for a layer of the matrix currently being processed. For example, the Layered Decoder Presentation discloses an R OLD SELECT unit that selects an R old message for a layer of the matrix currently being processed.



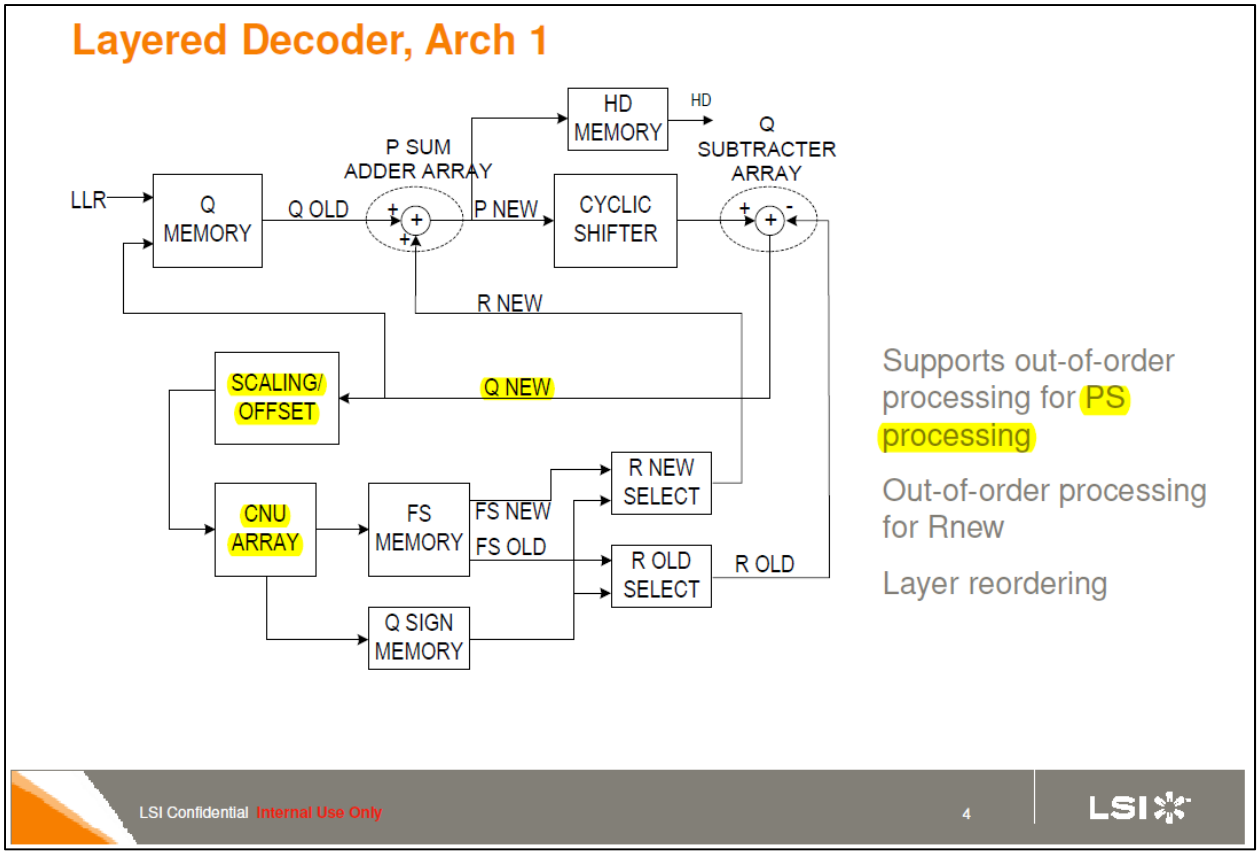
269. The Accused Products include a control unit configured to cause the decoding circuitry to process each block of the LDPC matrix in processing substeps comprising a P message substep that generates updated P messages. For example, the Layered Decoder Presentation discloses a P NEW message created by combining the Q OLD message and the R NEW message together.



270. The Accused Products include a control unit configured to cause the decoding circuitry to process each block of the LDPC matrix in processing substeps comprising a Q message substep that computes variable node messages (Q messages). For example, the Layered Decoder Presentation discloses a Q SUBTRACTER ARRAY that computes variable node messages (Q messages).



271. The Accused Products include a control unit configured to cause the decoding circuitry to process each block of the LDPC matrix in processing substeps comprising a partial state substep that updates partial state of a block row based on Q messages computed for the block (check node unit (CNU) Partial state processing). For example, the Layered Decoder Presentation discloses a partial state substep that updates the partial state of a block row based on Q messages computed for the block (check node unit (CNU) Partial state processing).



272. Claim 9 of the ’950 patent recites as follows:

9. A method comprising:
processing blocks of a layer of a low density parity check (LDPC) matrix out of order, the processing of each of the blocks comprising:
an R new update step comprising providing an R new message, the R new message produced for a block of a different layer of the matrix from a layer containing a block currently being processed;
an R old update step comprising selecting an R old message, the R old message produced for a layer of the matrix currently being processed;
a P message step comprising generating updated P messages;
a Q message step comprising computing variable node messages (Q messages); and
a partial state step comprising updating partial state of a block row based on Q messages computed for the block (check node unit (CNU) Partial state processing).

273. On information and belief, the Accused Products satisfy each and every limitation of Claim 9. The Accused Products process blocks of a layer of an LDPC matrix out of order. *See* ¶ 266, 99, 91, *supra*.

274. The Accused Products process each of the blocks comprising an R new update step comprising providing an R new message, the R new message produced for a block of a different layer of the matrix from a layer containing a block currently being processed. *See* ¶ 266, 137, 91, *supra*.

275. The Accused Products process each of the blocks comprising an R old update step comprising selecting an R old message, the R old message produced for a layer of the matrix currently being processed. *See* ¶ 266, 138, 91, *supra*.

276. The Accused Products process each of the blocks comprising a P message step comprising generating updated P messages. *See* ¶ 266, 263, 91, *supra*.

277. The Accused Products process each of the blocks comprising a Q message step comprising computing variable node messages (Q messages). *See* ¶ 266, 91, *supra*.

278. The Accused Products process each of the blocks comprising a partial state step comprising updating partial state of a block row based on Q messages computed for the block (check node unit (CNU) Partial state processing). *See* ¶¶ 266, 265, 91, *supra*.

279. In view of the foregoing, Defendant directly infringes at least Claims 1-16 of the ’950 patent through its internal testing, use, and operation of the Accused Products.

280. On information and belief, Defendant should have known that it directly infringes as of the date the ’950 patent issued on or about November 27, 2018, and in any event at least as early as the filing and/or service of this Complaint. Defendant is further aware that the Accused Products necessarily practice Claims 1-16 of the ’950 patent.

281. On information and belief, Defendant takes active steps to induce infringement by others of at least Claims 1-16 of the '950 patent in violation of 35 U.S.C. §271(b), including, for example, by (a) inducing manufacturers to perform the claimed inventions when testing the Accused Products, and (b) inducing end users to perform the claimed inventions when using the Accused Products. Such active steps include, but are not limited to, selling Accused Products with the knowledge and intent that the Accused Products will be operated by such manufacturers and their customers in accordance with the claimed inventions.

282. On information and belief, Defendant knows or should know that such activities induce others to directly infringe one or more of at least claims 1-16 of the '950 patent. For example, Defendant should have known that its actions induced others to directly infringe as of the date it became aware of the issuance of the '950 patent on or about November 27, 2018. Defendant was further informed that the technology in the Accused Products infringed the '950 patent, and Defendant knowingly and purposefully continued to exploit the patented technology despite knowing that it was covered by the '950 patent.

283. On information and belief, Defendant contributes to the infringement of at least Claims 1-16 of the '950 patent by others, including consumer/end-user use of the Accused Products, in violation of 35 U.S.C. § 271(c). Acts by Defendant that contribute to the infringement of others include, but are not limited to, the sale, offer for sale, and/or import by Defendant of the Accused Products. Such Accused Products are especially made for or adapted for use to infringe, and are not a staple article of commerce and are not suitable for substantial non-infringing use. The Accused Products are apparatuses for use in practicing Claims 1-16 of the '950 patent and are at least a material part of those claimed inventions, for example, as described above with respect to claim 9. On information and belief, the steps recited in Claim 9,

for example, are performed by the Accused Products. As also described above, Defendant has, on information and belief, been on notice of the '950 patent since it issued on November 27, 2018, and in addition since filing and/or service of this Complaint, and defendant has further been aware that use of the Accused Products necessarily practice the inventions in Claims 1-16 of the '950 patent.

284. The Accused Products are especially made for or adapted for use to infringe, and are not a staple article of commerce and are not suitable for substantial non-infringing use. By way of example, the use of the LDPC decoders included in the Accused Products is necessary to use the accused products for their intended purpose (decoding data from a hard disk drive, solid state drive, or wireless digital transmission), and the LDPC decoders necessarily perform the claimed inventions when they decode data. Accordingly, the Accused Products do not have a substantial use that does not entail practicing the claimed inventions. On information and belief, the Accused Products cannot be used but to infringe the '950 patent.

285. Despite Defendant's knowledge, notice, and ongoing infringement of the '950 patent, Defendant continues to test or use the Accused Products in a manner that willfully infringes the '950 patent, and on information and belief continues to sell and/or offer for sale the Accused Products to the United States market for customers / end users to infringe. Defendant's infringement of the '950 patent is willful, as set forth above. Defendant lacks a justifiable belief that it does not infringe the '950 patent, or that the '950 patent is invalid or unenforceable, and has acted recklessly in its infringing activity, justifying an increase in the damages to be awarded to Plaintiff up to three times the amount found or assessed, in accordance with 35 U.S.C. § 284.

286. On information and belief, Defendant had actual or constructive knowledge of the '950 patent since at least November 27, 2018, and in any event no later than the filing and/or

service of this Complaint. Defendant knows or should know as of the date of filing and/or service of the Complaint that its actions induced others to directly infringe the '950 patent and contributed to infringement of the '950 patent.

287. This case is rendered an exceptional case at least in light of Defendant's willful infringement of the '950 patent, justifying an award to Plaintiff of its reasonable attorney fees, in accordance with 35 U.S.C. § 285.

288. Defendant has no adequate remedy at law for Defendant's acts of infringement. As a direct and proximate result of Defendant's acts of infringement, Plaintiff has suffered and continues to suffer damages and irreparable harm. Unless Defendant's acts of infringement are enjoined by this Court, Plaintiff will continue to be damaged and irreparably harmed.

289. Defendant's infringement of the '950 patent has damaged and continues to damage Plaintiff in an amount yet to be determined, of at least a reasonable royalty and/or lost profits that Plaintiff would have made but for Defendant's infringement acts.

COUNT VII
(Copyright Infringement under 17 U.S.C. §§ 106 and 501, *et seq.* of "Low Density Parity Check Decoder", U.S. Copyright Registration No. TXu 2-001-020)

290. Plaintiff repeats and re-alleges the paragraphs above as if fully set forth herein.

291. TAMUS is the owner of the copyright in the LDPC Decoder Program Work, which is the subject of U.S. Copyright Registration No. TXu 2-001-020. TAMUS has granted Plaintiff an exclusive licensee to reproduce, distribute, publicly display and perform, and make derivative works from the LDPC Decoder Program Work, grant sublicenses thereto, and to sue for infringement of the copyrights in the LDPC Decoder Program Work.

292. Upon information and belief, Defendant has violated Plaintiff's exclusive rights in the LDPC Decoder Program Work by, for example, continuing to use copies of the LDPC Decoder Program Work, or copies of works that are derivative works of the LDPC Decoder Program Work, in its ongoing engineering and design of the Accused Products, thereby violating Plaintiff's exclusive rights to (a) make reproductions of the LDPC Decoder Program Work or parts thereof, and (b) make derivative works from the LDPC Decoder Program Work.

293. The acts of Defendant constitute copyright infringement under 17 U.S.C. §§ 106 and 501, *et seq.*

294. Defendant will continue to infringe Plaintiff's exclusive rights with respect to the LDPC Decoder Program Work unless permanently enjoined by this Court.

295. Defendant's infringement has been willful and purposeful.

296. Plaintiff has been and continues to be damaged by Defendant's acts of infringement, and Plaintiff is entitled to a permanent injunction and an award of its actual damages and any profits of Defendant under 17 U.S.C. §§ 502, 504(a)(1), and 504(b).

297. Upon information and belief, the infringing acts of Defendant were undertaken and/or continue with knowledge of the Plaintiff's rights and without any good faith basis in law or fact that Defendant's actions were legal, thus Defendant's infringing acts were committed willfully and with reckless disregard of Plaintiff's known rights.

COUNT VIII
(Copyright Infringement under 17 U.S.C. §§ 106 and 501, *et seq.* of "Source Code for Low Density Parity Check Decoder and Its Modules", U.S. Copyright Registration No. TXu 2-033-302)

298. Plaintiff repeats and re-alleges the paragraphs above as if fully set forth herein.

299. TAMUS is the owner of the copyright in the LDPC Decoder Source Code Work, which is the subject of U.S. Copyright Registration No. TXu 2-033-302. TAMUS has granted Plaintiff an exclusive licensee to reproduce, distribute, publicly display and perform, and make derivative works from the LDPC Decoder Source Code Work, grant sublicenses thereto, and to sue for infringement of the copyrights in the LDPC Decoder Source Code Work.

300. Upon information and belief, Defendant has violated Plaintiff's exclusive rights in the LDPC Decoder Source Code Work by, for example, continuing to use copies of the LDPC Decoder Source Code Work, or copies of works that are derivative works of the LDPC Decoder Source Code Work, in its ongoing engineering and design of the Accused Products, thereby violating Plaintiff's exclusive rights to (a) make reproductions of the LDPC Decoder Source Code Work or parts thereof, and (b) make derivative works from the LDPC Decoder Source Code Work.

301. The acts of Defendant constitute copyright infringement under 17 U.S.C. §§ 106 and 501, *et seq.*

302. Defendant will continue to infringe Plaintiff's exclusive rights with respect to the LDPC Decoder Source Code Work unless permanently enjoined by this Court.

303. Defendant's infringement has been willful and purposeful.

304. Plaintiff has been and continues to be damaged by Defendant's acts of infringement, and Plaintiff is entitled to a permanent injunction and an award of its actual damages and any profits of Defendant under 17 U.S.C. §§ 502, 504(a)(1), and 504(b).

305. Upon information and belief, the infringing acts of Defendant were undertaken and/or continue with knowledge of the Plaintiff's rights and without any good faith basis in law or fact that Defendant's actions were legal, thus Defendant's infringing acts were committed willfully and with reckless disregard of Plaintiff's known rights.

COUNT IX
(Copyright Infringement under 17 U.S.C. §§ 106 and 501, *et seq.* of "Source Code for Certain Low Density Parity Check Algorithms", U.S. Copyright Registration No. TXu 1-842-620)

306. Plaintiff repeats and re-alleges the paragraphs above as if fully set forth herein.

307. TAMUS is the owner of the copyright in the LDPC Algorithms Source Code Work, which is the subject of U.S. Copyright Registration No. TXu 1-842-620. TAMUS has granted Plaintiff an exclusive licensee to reproduce, distribute, publicly display and perform, and make derivative works from the LDPC Decoder Source Code Work, grant sublicenses thereto, and to sue for infringement of the copyrights in the LDPC Decoder Source Code Work.

308. Upon information and belief, Defendant has violated Plaintiff's exclusive rights in the LDPC Algorithms Source Code Work by, for example, continuing to use copies of the LDPC Algorithms Source Code Work, or copies of works that are derivative works of the LDPC Algorithms Source Code Work, in its ongoing engineering and design of the Accused Products, thereby violating Plaintiff's exclusive rights to (a) make reproductions of the LDPC Algorithms Source Code Work or parts thereof, and (b) make derivative works from the LDPC Algorithms Source Code Work.

309. The acts of Defendant constitute copyright infringement under 17 U.S.C. §§ 106 and 501, *et seq.*

310. Defendant's infringement has been willful and purposeful.

311. Defendant will continue to infringe Plaintiff's exclusive rights with respect to the LDPC Algorithms Source Code Work unless permanently enjoined by this Court.

312. Plaintiff has been and continues to be damaged by Defendant's acts of infringement, and Plaintiff is entitled to a permanent injunction and an award of its actual damages and any profits of Defendant under 17 U.S.C. §§ 502, 504(a)(1), and 504(b).

313. Upon information and belief, the infringing acts of Defendant were undertaken and/or continue with knowledge of the Plaintiff's rights and without any good faith basis in law or fact that Defendant's actions were legal, thus Defendant's infringing acts were committed willfully and with reckless disregard of Plaintiff's known rights.

JURY TRIAL DEMAND

Pursuant to Federal Rule of Civil Procedure 38(b), Plaintiff hereby demands a trial by jury of all issues so triable.

REQUESTED RELIEF

Plaintiff respectfully seeks the following relief:

a) The entry of judgment holding that Defendant has infringed each of the '023, '140, '530, '522, '250, and '950 Patents;

b) The entry of a permanent injunction pursuant to 35 U.S.C. § 283 enjoining Defendant, its officers, agents, attorneys, and employees, and those acting or attempting to act in active concert with them or acting on their behalf, from infringing any of the ’023, ’140, ’530,’522, ’250 and ’950 Patents by engaging in any commercial manufacture, use, offer to sell, or sale within the United States, or importation into the United States, of any product covered by the ’023, ’140, ’530, ’522, ’250, and ’950 Patents for the full terms thereof or any additional period of exclusivity to which Plaintiffs and/or such Patents are, or become, entitled, and from inducing or contributing to such activities;

c) The entry of an order declaring that Plaintiff be awarded damages in an amount sufficient to compensate it for Defendant’s infringement of the ’023, ’140,’530, ’522, ’250, and ’950 Patents, together with prejudgment and postjudgment interest and costs;

d) The entry of an order declaring that Plaintiff be awarded enhanced damages pursuant to 35 U.S.C. § 284 for Defendant’s willful patent infringement;

e) That Defendant be ordered to provide an accounting for the damages resulting from infringement of the Patents-in-Suit, together with interests and costs, and all other damages permitted by 35 U.S.C. § 284 (2012), including an accounting for infringing acts not presented at trial and an award by the court of additional damages for any such infringing acts.

f) The entry of an injunction, pursuant to 17 U.S.C. § 502, permanently enjoining Defendant from reproducing, publishing, posting, copying, offering to copy, or otherwise distributing, and from making any derivative works of, the TAMUS Copyrighted Works, including all versions thereof;

g) Award Plaintiff its damages, in addition to Defendant’s profits, as a result of Defendant’s acts of copyright infringement;

h) That Defendant be ordered to provide an accounting for the damages resulting from infringement of the of Copyrights-in-suit, and all other damages permitted by 17 U.S.C. § 504, including an accounting for infringing acts not presented at trial and an award by the court of additional damages for any such infringing acts;

i) In the alternative, and if Plaintiff so elects, award Plaintiff statutory damages pursuant to 17 U.S.C. § 504, *et seq.* per each of the Copyrighted Works infringed by Defendant, including damages on account of Defendant's willful infringement of the Copyrighted Works.

j) The entry of an order declaring that this is an exceptional case and awarding Plaintiff its costs, expenses, and reasonable attorney fees under 35 U.S.C. § 285 and 17 U.S.C. § 505 and all other applicable statutes, rules, and common law;

k) The taxation of all allowable costs against Defendant; and

l) An award to Plaintiff of any other relief that the Court deems just and proper under the circumstances.

Dated: December 12, 2018

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